



Is Now Part of



ON Semiconductor®

To learn more about ON Semiconductor, please visit our website at
www.onsemi.com

ON Semiconductor and the ON Semiconductor logo are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.



FDMF3030 — Extra-Small, High-Performance, High-Frequency, DrMOS Module

Benefits

- Ultra-Compact 6x6mm PQFN, 72% Space-Saving Compared to Conventional Discrete Solutions
- Fully Optimized for System Efficiency
- Clean-Switching Waveforms with Minimal Ringing
- High-Current Handling

Features

- Over 93% Peak-Efficiency
- High-Current Handling: 50A
- High-Performance PQFN Copper-Clip Package
- 3-State 5V PWM Input Driver
- Automatic Diode Emulation (Skip Mode) Enabled through ZCD_EN# Input
- Thermal Warning Flag for Over-Temperature Condition
- Driver Output Disable Function (DISB# Pin)
- Internal Pull-Up and Pull-Down for ZCD_EN# and DISB# Inputs, Respectively
- Fairchild PowerTrench® Technology MOSFETs for Clean Voltage Waveforms and Reduced Ringing
- Fairchild SyncFET™ Technology (Integrated Schottky Diode) in Low-Side MOSFET
- Integrated Bootstrap Schottky Diode
- Adaptive Gate-Drive Timing for Shoot-Through Protection
- Under-Voltage Lockout (UVLO)
- Optimized for Switching Frequencies up to 1MHz
- Low-Profile SMD Package
- Fairchild Green Packaging and RoHS Compliance
- Based on the Intel® 4.0 DrMOS Standard

Description

The DrMOS family is Fairchild's next-generation, fully optimized, ultra-compact, integrated MOSFET-plus-driver, power-stage solution for high-current, high-frequency, synchronous buck, DC-DC applications. The FDMF3030 integrates a driver IC, two power MOSFETs, and a bootstrap Schottky diode into a thermally enhanced, ultra-compact, 6x6mm package.

With an integrated approach, the complete switching power stage is optimized with regard to driver and MOSFET dynamic performance, system inductance, and power MOSFET $R_{DS(ON)}$. The FDMF3030 uses Fairchild's high-performance PowerTrench® MOSFET technology, which dramatically reduces switch ringing, eliminating the need for a snubber circuit in most buck converter applications.

A driver IC with reduced dead times and propagation delays further enhances performance. A thermal warning function indicates a potential over-temperature situation. The FDMF3030 also incorporates a Zero-Cross Detect (ZCD_EN# pin) for improved light-load efficiency and provides a 3-state 5V PWM input for compatibility with a wide range of PWM controllers.

Applications

- Notebook Computers
- High-Performance Gaming Motherboards
- Compact Blade Servers & Workstations, V-Core and Non-V-Core DC-DC Converters
- Desktop Computers, V-Core and Non-V-Core DC-DC Converters
- High-Current DC-DC Point-of-Load Converters
- Networking and Telecom Microprocessor Voltage Regulators
- Small Form-Factor Voltage Regulator Modules

Ordering Information

Part Number	Current Rating	Package	Top Mark
FDMF3030	50A	40-Lead, Clipbond PQFN DrMOS, 6.0mm x 6.0mm Package	FDMF3030

Typical Application Circuit

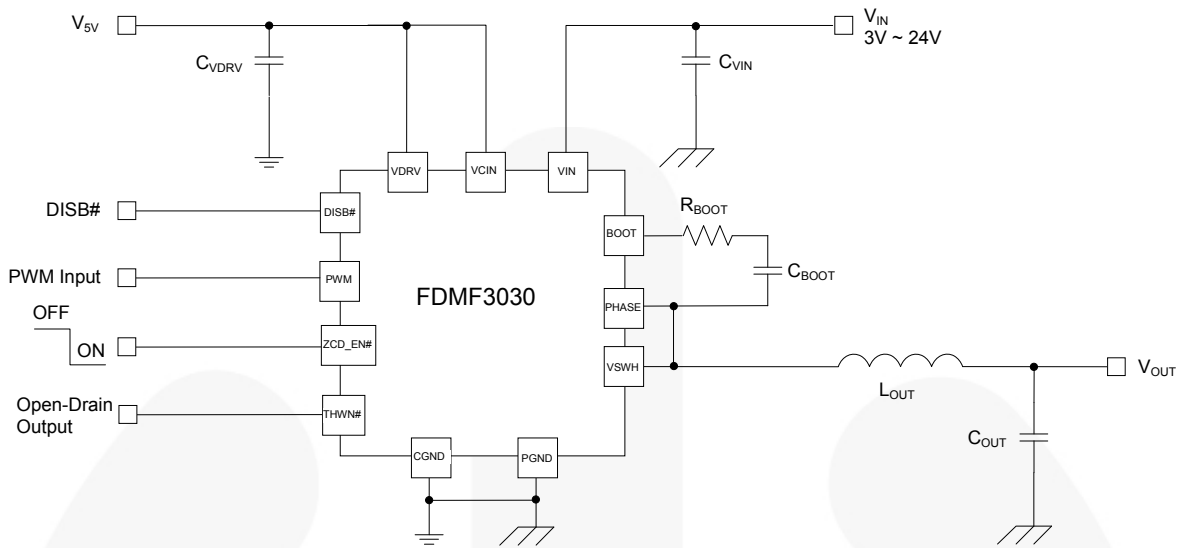


Figure 1. Typical Application Circuit

DrMOS Block Diagram

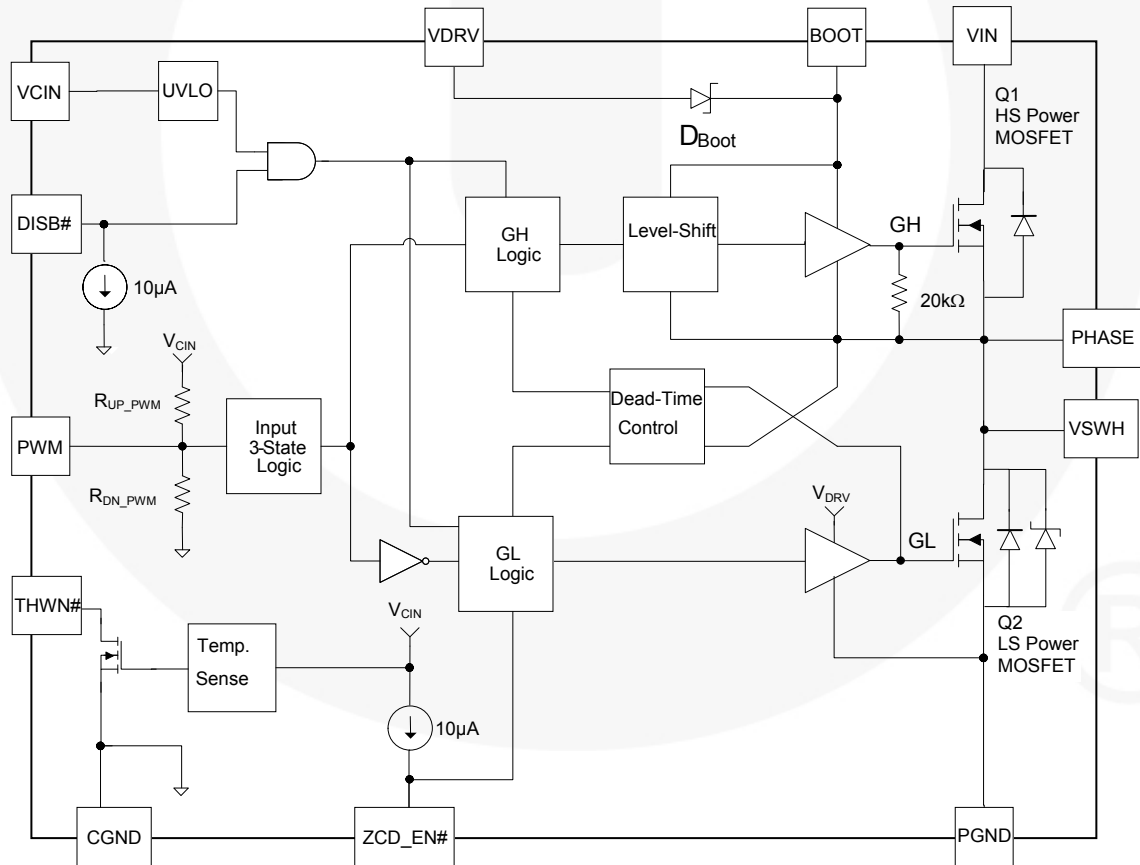


Figure 2. DrMOS Block Diagram

Pin Configuration

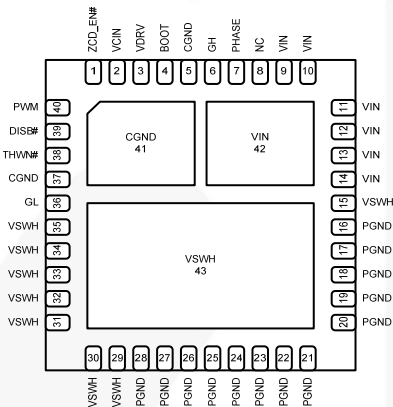
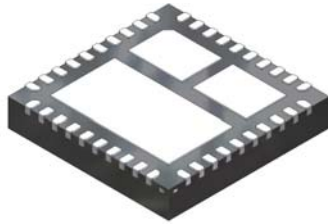


Figure 3. Bottom View

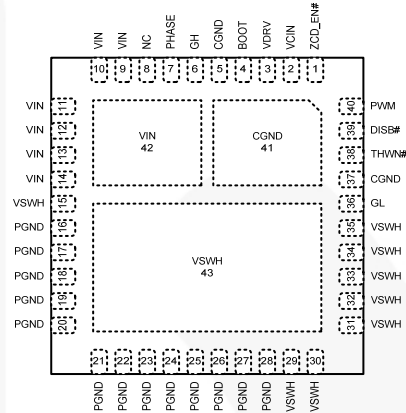
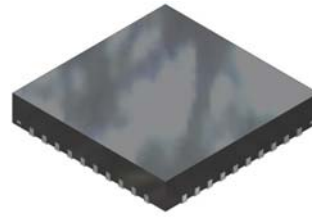


Figure 4. Top View

Pin Definitions

Pin #	Name	Description
1	ZCD_EN#	When ZCD_EN#=HIGH, the low-side driver is the inverse of the PWM input. When ZCD_EN#=LOW, diode emulation is enabled. This pin has a 10 μ A internal pull-up current source. Do not add a noise filter capacitor.
2	VCIN	IC bias supply. Minimum 1 μ F ceramic capacitor is recommended from this pin to CGND.
3	VDRV	Power for the gate driver. Minimum 1 μ F ceramic capacitor is recommended to be connected as close as possible from this pin to CGND.
4	BOOT	Bootstrap supply input. Provides voltage supply to the high-side MOSFET driver. Connect a bootstrap capacitor from this pin to PHASE.
5, 37, 41	CGND	IC ground. Ground return for driver IC.
6	GH	For manufacturing test only. This pin must float; it must not be connected to any pin.
7	PHASE	Switch node pin for bootstrap capacitor routing. Electrically shorted to VSWH pin.
8	NC	No connect. The pin is not electrically connected internally, but can be connected to VIN for convenience.
9 - 14, 42	VIN	Power input. Output stage supply voltage.
15, 29 - 35, 43	VSWH	Switch node input. Provides return for high-side bootstrapped driver and acts as a sense point for the adaptive shoot-through protection.
16 - 28	PGND	Power ground. Output stage ground. Source pin of the low-side MOSFET.
36	GL	For manufacturing test only. This pin must float; it must not be connected to any pin.
38	THWN#	Thermal warning flag, open collector output. When temperature exceeds the trip limit, the output is pulled LOW. THWN# does not disable the module.
39	DISB#	Output disable. When LOW, this pin disables power MOSFET switching (GH and GL are held LOW). This pin has a 10 μ A internal pull-down current source. Do not add a noise filter capacitor.
40	PWM	PWM signal input. This pin accepts a three-state 5V PWM signal from the controller.

Absolute Maximum Ratings

Stresses exceeding the Absolute Maximum Ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V _{CIN}	Supply Voltage	Referenced to CGND	-0.3	7.0	V
V _{DRV}	Drive Voltage	Referenced to CGND	-0.3	7.0	V
V _{DISB#}	Output Disable	Referenced to CGND	-0.3	7.0	V
V _{PWM}	PWM Signal Input	Referenced to CGND	-0.3	7.0	V
V _{ZCD_EN#}	ZCD Enable Signal Input	Referenced to CGND	-0.3	7.0	V
V _{GL}	Low Gate Manufacturing Test Pin	Referenced to CGND	-0.3	7.0	V
V _{THWN#}	Thermal Warning Flag	Referenced to CGND	-0.3	7.0	V
V _{IN}	Power Input	Referenced to PGND, CGND	-0.3	30.0	V
V _{BOOT}	Bootstrap Supply	Referenced to VSWH, PHASE	-0.3	7.0	V
		Referenced to CGND	-0.3	30.0	V
V _{GH}	High Gate Manufacturing Test Pin	Referenced to VSWH, PHASE	-0.3	7.0	V
		Referenced to CGND	-0.3	30.0	V
V _{PHS}	PHASE	Referenced to CGND	-0.3	30.0	V
V _{SWH}	Switch Node Input	Referenced to PGND, CGND (DC Only)	-0.3	30.0	V
		Referenced to PGND, <20ns	-8.0	33.0	V
V _{BOOT}	Bootstrap Supply	Referenced to VDRV		22.0	V
		Referenced to VDRV, <20ns		25.0	V
I _{THWN#}	THWN# Sink Current		-0.1	7.0	mA
I _{O(AV)}	Output Current ⁽¹⁾	f _{SW} =300kHz, V _{IN} =12V, V _O =1.0V		50	A
		f _{SW} =1MHz, V _{IN} =12V, V _O =1.0V		45	
θ _{JPCB}	Junction-to-PCB Thermal Resistance (Fairchild Evaluation Board)			3	°C/W
T _A	Ambient Temperature Range		-40	+125	°C
T _J	Maximum Junction Temperature			+150	°C
T _{STG}	Storage Temperature Range		-55	+150	°C
ESD	Electrostatic Discharge Protection	Human Body Model, JESD22-A114	2000		V
		Charged Device Model, JESD22-C101	2000		

Note:

- I_{O(AV)} is rated using Fairchild's DrMOS evaluation board, at T_A = 25°C, with natural convection cooling. This rating is limited by the peak DrMOS temperature, T_J = 150°C, and varies depending on operating conditions and PCB layout. This rating can be changed with different application settings.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _{CIN}	Control Circuit Supply Voltage	4.5	5.0	5.5	V
V _{DRV}	Gate Drive Circuit Supply Voltage	4.5	5.0	5.5	V
V _{IN}	Output Stage Supply Voltage	3.0	12.0	24.0 ⁽²⁾	V

Note:

- Operating at high V_{IN} can create excessive AC overshoots on the VSWH-to-GND and BOOT-to-GND nodes during MOSFET switching transients. For reliable DrMOS operation, VSWH-to-GND and BOOT-to-GND must remain at or below the Absolute Maximum Ratings shown in the table above. Refer to the "Application Information" and "PCB Layout Guidelines" sections of this datasheet for additional information.

Electrical Characteristics

Typical values are $V_{IN} = 12V$, $V_{CIN} = 5V$, $V_{DRV} = 5V$, and $T_A = T_J = +25^\circ C$ unless otherwise noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Basic Operation						
I_Q	Quiescent Current	$I_Q = I_{VCIN} + I_{VDRV}$, PWM=LOW or HIGH or Float			2	mA
V_{UVLO}	UVLO Threshold	V_{CIN} Rising		3.3		V
V_{UVLO_HYS}	UVLO Hysteresis			0.35		V
PWM Input ($V_{CIN} = V_{DRV} = 5V \pm 10\%$)						
R_{UP_PWM}	Pull-Up Impedance	$V_{PWM}=5V$		20		k Ω
R_{DN_PWM}	Pull-Down Impedance	$V_{PWM}=0V$		20		k Ω
V_{IH_PWM}	PWM High Level Voltage		3.15	3.80	4.45	V
V_{TRI_HI}	3-State Upper Threshold		3.10	3.75	4.40	V
V_{TRI_LO}	3-State Lower Threshold		1.05	1.40	1.90	V
V_{IL_PWM}	PWM Low Level Voltage		0.70	1.00	1.30	V
$t_{D_HOLD-OFF}$	3-State Shut-Off Time			150		ns
V_{HIZ_PWM}	3-State Open Voltage		2.20	2.50	2.80	V
$t_{PWM-OFF_MIN}$	PWM Minimum Off Time		70			ns
PWM Input ($V_{CIN} = V_{DRV} = 5V \pm 5\%$)						
R_{UP_PWM}	Pull-Up Impedance	$V_{PWM}=5V$		20		k Ω
R_{DN_PWM}	Pull-Down Impedance	$V_{PWM}=0V$		20		k Ω
V_{IH_PWM}	PWM High Level Voltage		3.35	3.80	4.25	V
V_{TRI_HI}	3-State Upper Threshold		3.30	3.75	4.20	V
V_{TRI_LO}	3-State Lower Threshold		1.10	1.40	1.75	V
V_{IL_PWM}	PWM Low Level Voltage		0.74	1.00	1.26	V
$t_{D_HOLD-OFF}$	3-State Shut-Off Time			150		ns
V_{HIZ_PWM}	3-State Open Voltage		2.30	2.50	2.70	V
$t_{PWM-OFF_MIN}$	PWM Minimum Off Time		70			ns
DISB# Input						
V_{IH_DISB}	High-Level Input Voltage		2			V
V_{IL_DISB}	Low-Level Input Voltage				0.8	V
I_{PLD}	Pull-Down Current			10		μA
t_{PD_DISBL}	Propagation Delay	PWM=GND, Delay Between DISB# from HIGH to LOW to GL from HIGH to LOW		220		ns
t_{PD_DISBH}	Propagation Delay	PWM=GND, Delay Between DISB# from LOW to HIGH to GL from LOW to HIGH		520		ns
ZCD_EN# Input						
$V_{IH_ZCD_EN}$	High-Level Input Voltage		2			V
$V_{IL_ZCD_EN}$	Low-Level Input Voltage				0.8	V
I_{PLU}	Pull-Up Current			10		μA
t_{PD_ZLGLL}	Propagation Delay	PWM=GND, Delay Between ZCD_EN# from HIGH to LOW to GL from HIGH to LOW		1800		ns
t_{PD_ZHGLH}	Propagation Delay	PWM=GND, Delay Between ZCD_EN# from LOW to HIGH to GL from LOW to HIGH		20		ns

Continued on the following page...

Electrical Characteristics

Typical values are $V_{IN} = 12V$, $V_{CIN} = 5V$, $V_{DRV} = 5V$, and $T_A = T_J = +25^{\circ}C$ unless otherwise noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Thermal Warning Flag						
T_{ACT}	Activation Temperature			150		$^{\circ}C$
T_{RST}	Reset Temperature			135		$^{\circ}C$
R_{THWN}	Pull-Down Resistance	5k Ω Resistor Pull-up to V_{CIN}		60		Ω
High-Side Driver ($f_{sw} = 1000kHz$, $I_{OUT} = 30A$, $T_A = +25^{\circ}C$)						
R_{SOURCE_GH}	Output Impedance, Sourcing	Source Current=50mA		0.8		Ω
R_{SINK_GH}	Output Impedance, Sinking	Sink Current=50mA		0.6		Ω
t_{R_GH}	Rise Time	GH=10% to 90%		10		ns
t_{F_GH}	Fall Time	GH=90% to 10%		10		ns
t_{D_DEADON}	LS to HS Deadband Time	GL Going LOW to GH Going HIGH, 1.7V GL to 10% GH		20		ns
t_{PD_PLGHL}	PWM LOW Propagation Delay	PWM Going LOW to GH Going LOW, V_{IL_PWM} to 90% GH		20		ns
t_{PD_PHGHH}	PWM HIGH Propagation Delay (ZCD_EN# =0)	PWM Going HIGH to GH Going HIGH, V_{IH_PWM} to 10% GH (ZCD_EN# =0, $I_{D_LS}>0$)		25		ns
t_{PD_TSGHH}	Exiting 3-State Propagation Delay	PWM (From 3-State) Going HIGH to GH Going HIGH, V_{IH_PWM} to 10% GH		35		ns
Low-Side Driver ($f_{sw} = 1000kHz$, $I_{OUT} = 30A$, $T_A = +25^{\circ}C$)						
R_{SOURCE_GL}	Output Impedance, Sourcing	Source Current=50mA		0.9		Ω
R_{SINK_GL}	Output Impedance, Sinking	Sink Current=50mA		0.4		Ω
t_{R_GL}	Rise Time	GL=10% to 90%		15		ns
t_{F_GL}	Fall Time	GL=90% to 10%		10		ns
$t_{D_DEADOFF}$	HS to LS Deadband Time	SW Going LOW to GL Going HIGH, 1.7V SW to 10% GL		20		ns
t_{PD_PHGLL}	PWM-HIGH Propagation Delay	PWM Going HIGH to GL Going LOW, V_{IH_PWM} to 90% GL		20		ns
t_{PD_TSGLH}	Exiting 3-State Propagation Delay	PWM (From 3-State) Going LOW to GL Going HIGH, V_{IL_PWM} to 10% GL		30		ns
$t_{GL_ON_MIN}$	GL Minimum On Time in DCM	$V_{ZCD_EN\#}=0V$		350		ns
Boot Diode						
V_F	Forward-Voltage Drop	$I_F=1mA$		0.6		V
V_R	Breakdown Voltage	$I_R=1mA$	22			V

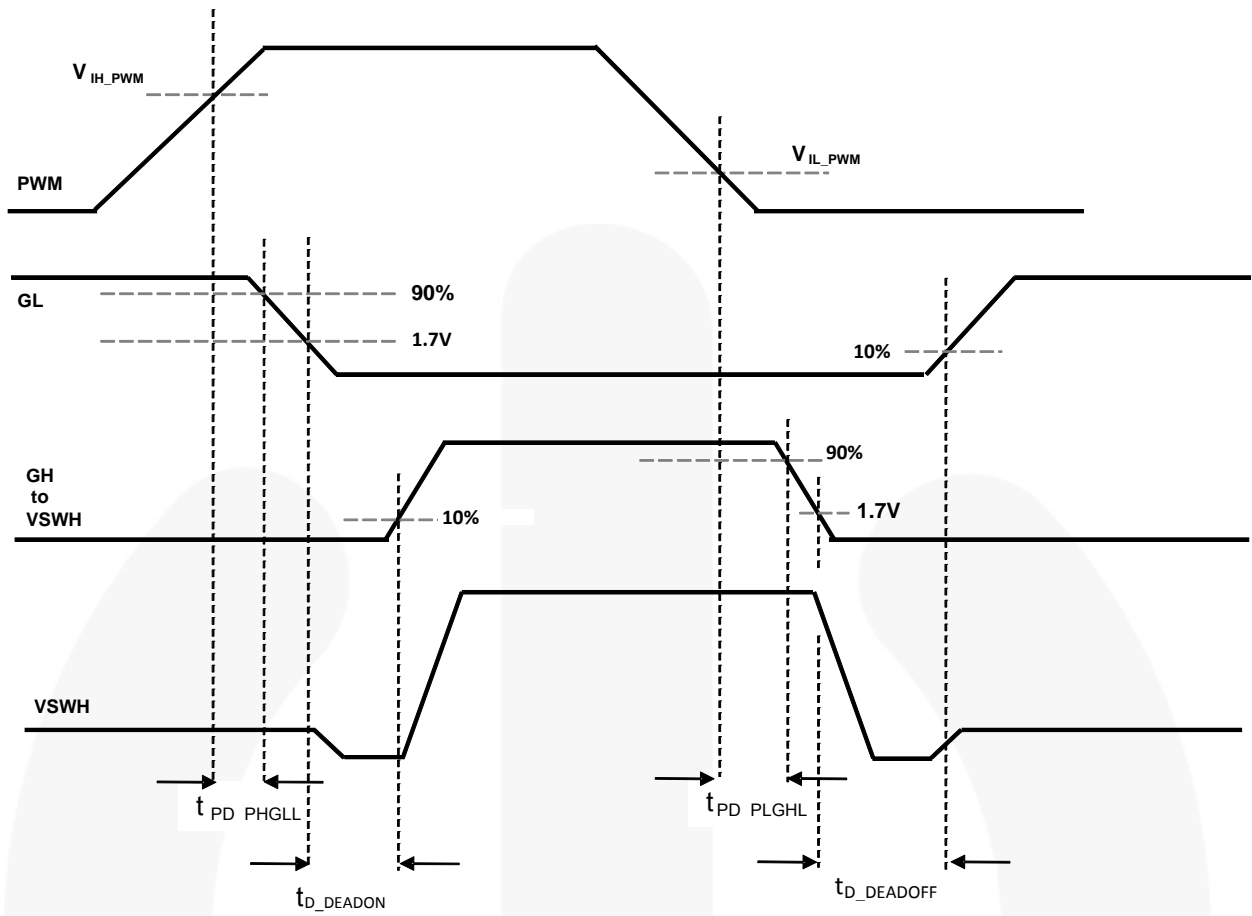


Figure 5. PWM Timing Diagram

Typical Performance Characteristics

Test Conditions: $V_{IN}=12V$ or $19V$, $V_{OUT}=1V$, $V_{CIN}=5V$, $V_{DRV}=5V$, $L_{OUT}=250nH$, $T_A=25^{\circ}C$, and natural convection cooling, unless otherwise specified.

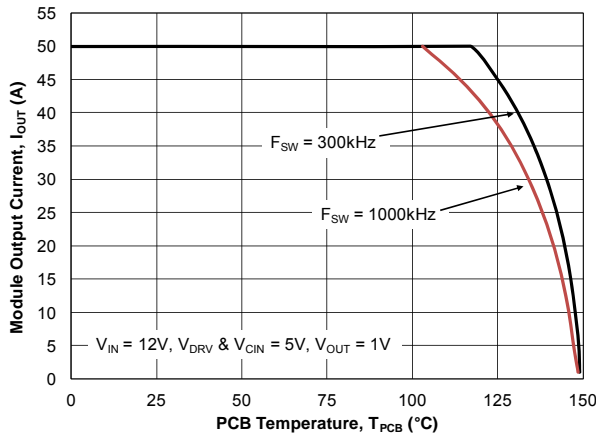


Figure 6. Safe Operating Area for 12V_{IN}

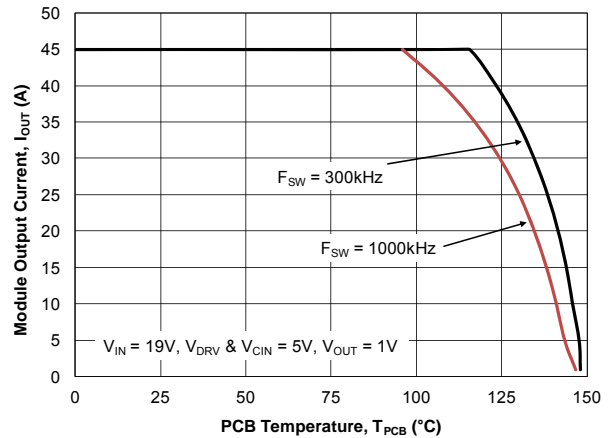


Figure 7. Safe Operating Area for 19V_{IN}

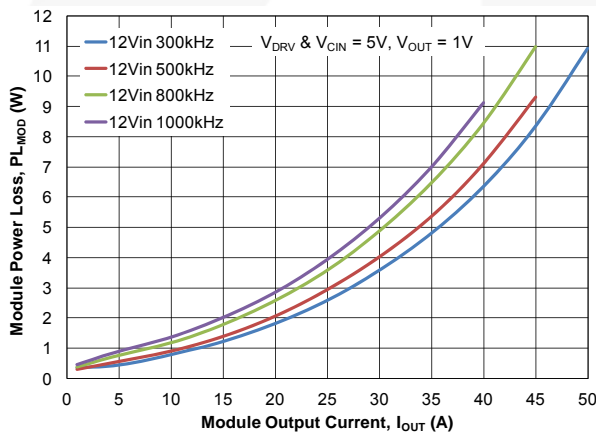


Figure 8. Power Loss vs. Output Current for 12V_{IN}

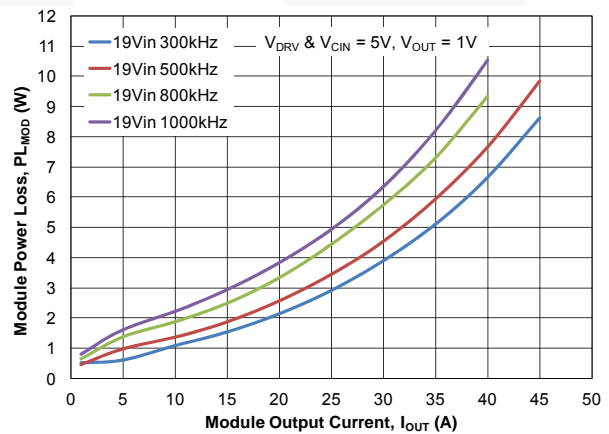


Figure 9. Power Loss vs. Output Current for 19V_{IN}

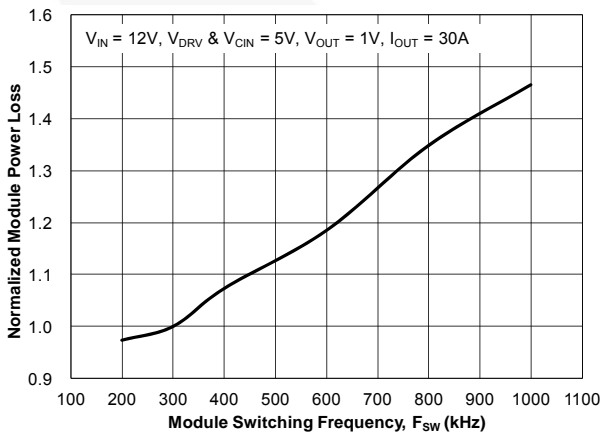


Figure 10. Power Loss vs. Switching Frequency

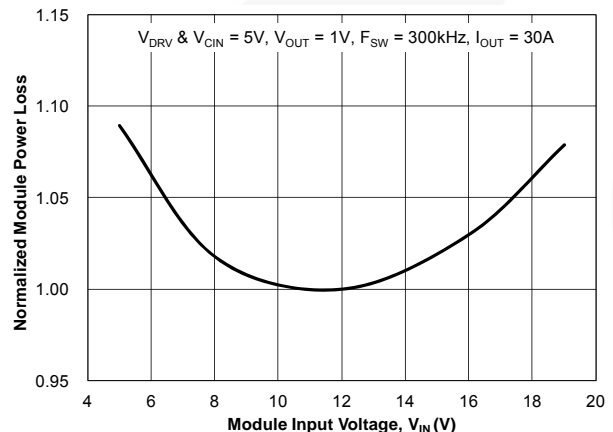


Figure 11. Power Loss vs. Input Voltage

Typical Performance Characteristics

Test Conditions: $V_{IN}=12V$, $V_{OUT}=1V$, $V_{CIN}=5V$, $V_{DRV}=5V$, $L_{OUT}=250nH$, $T_A=25^{\circ}C$, and natural convection cooling, unless otherwise specified.

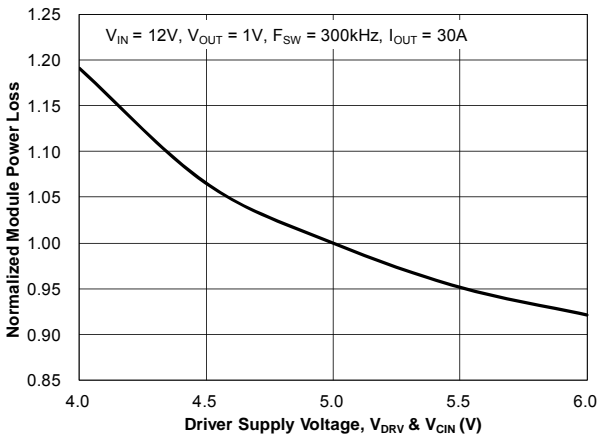


Figure 12. Power Loss vs. Driver Supply Voltage

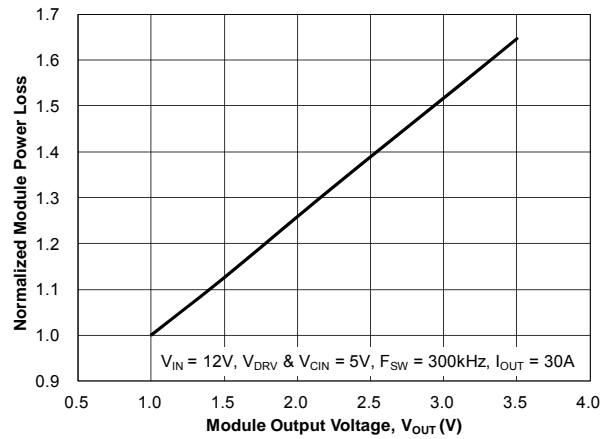


Figure 13. Power Loss vs. Output Voltage

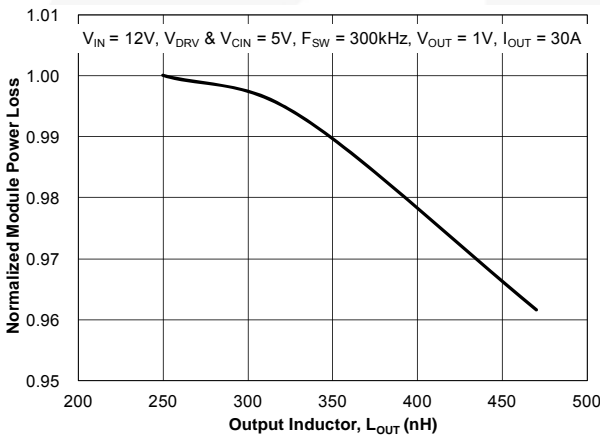


Figure 14. Power Loss vs. Output Inductor

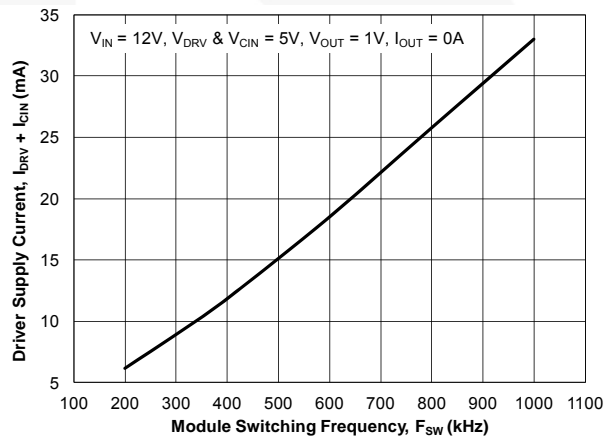


Figure 15. Driver Supply Current vs. Switching Frequency

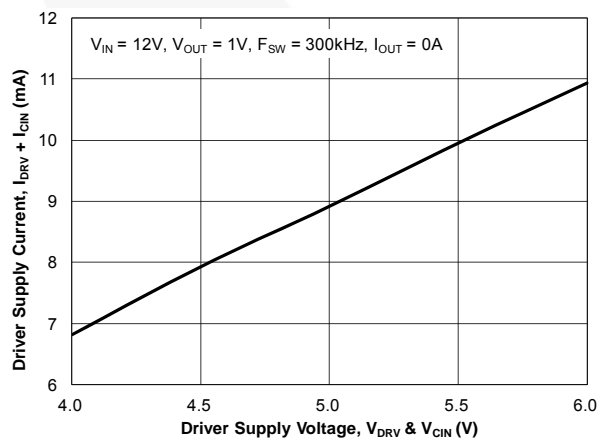


Figure 16. Driver Supply Current vs. Driver Supply Voltage

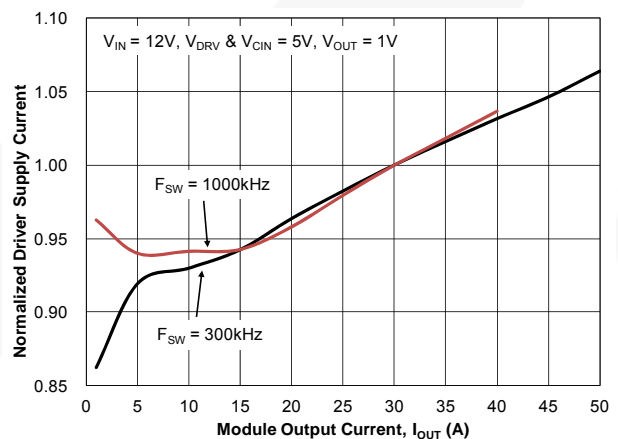


Figure 17. Driver Supply Current vs. Output Current

Typical Performance Characteristics

Test Conditions: $V_{CIN}=5V$, $V_{DRV}=5V$, $T_A=25^\circ C$, and natural convection cooling, unless otherwise specified.

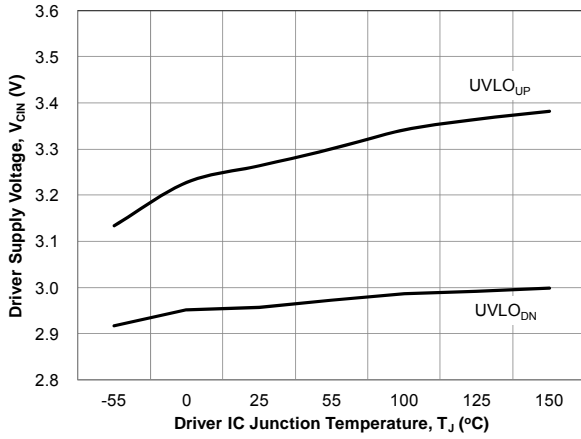


Figure 18. UVLO Threshold vs. Temperature

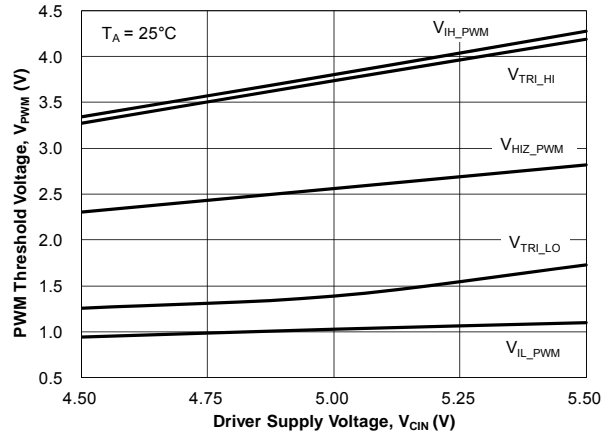


Figure 19. PWM Threshold vs. Driver Supply Voltage

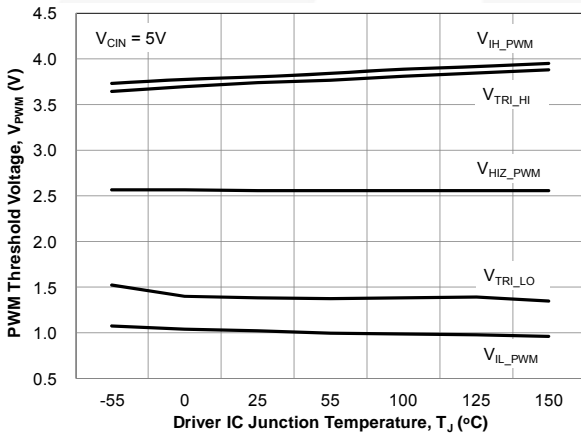


Figure 20. PWM Threshold vs. Temperature

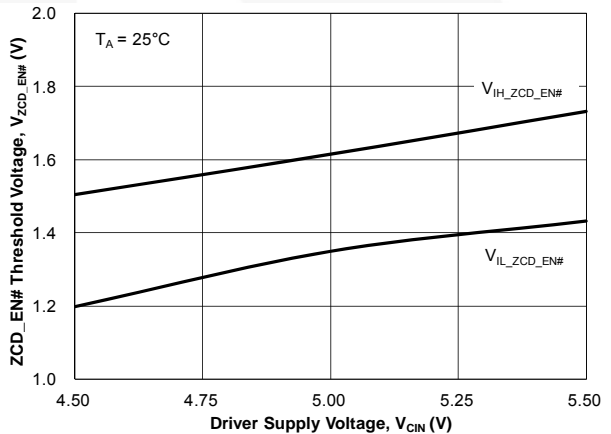


Figure 21. ZCD_EN# Threshold vs. Driver Supply Voltage

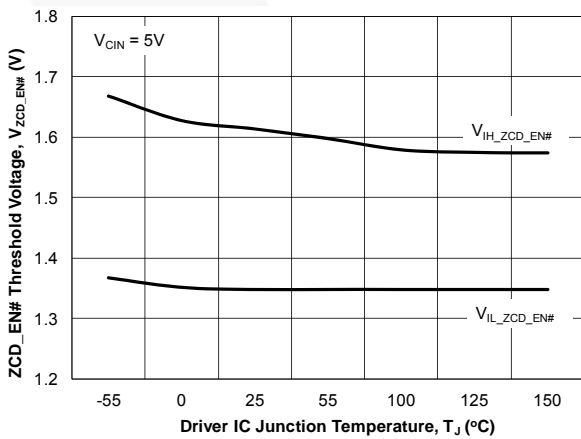


Figure 22. ZCD_EN# Threshold vs. Temperature

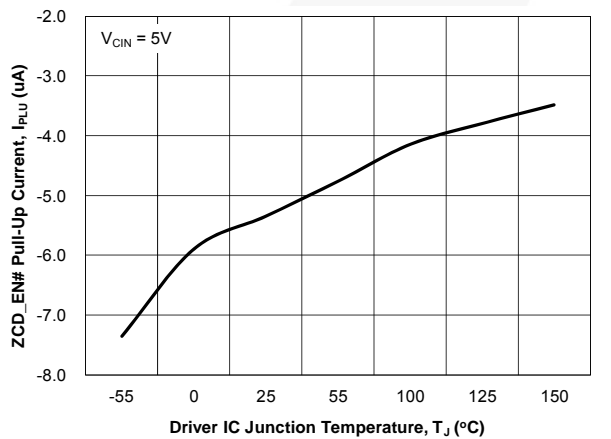


Figure 23. ZCD_EN# Pull-Up Current vs. Temperature

Typical Performance Characteristics

Test Conditions: $V_{CIN}=5V$, $V_{DRV}=5V$, $T_A=25^\circ C$, and natural convection cooling, unless otherwise specified.

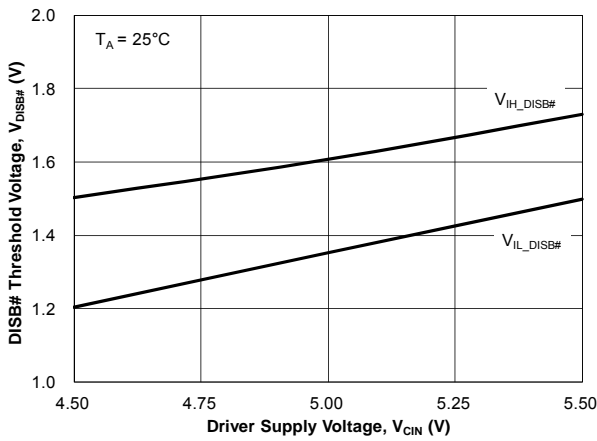


Figure 24. DISB# Threshold vs. Driver Supply Voltage

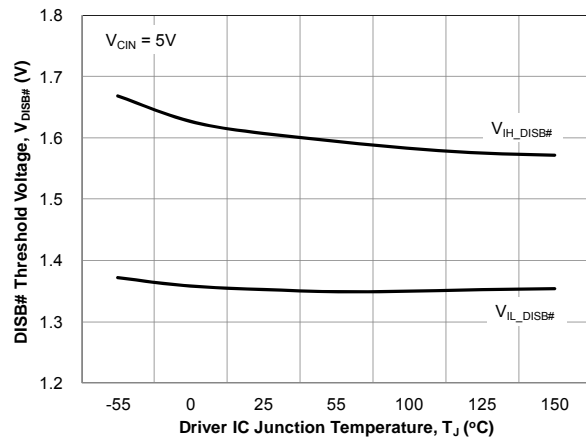


Figure 25. DISB# Threshold vs. Temperature

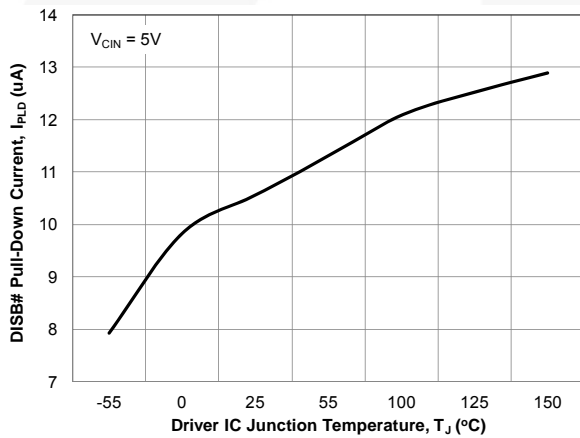


Figure 26. DISB# Pull-Down Current vs. Temperature

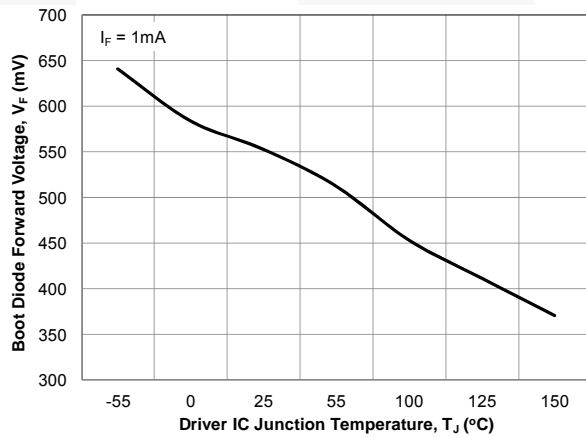


Figure 27. Boot Diode Forward Voltage vs. Temperature

Functional Description

The FDMF3030 is a driver-plus-FET module optimized for the synchronous buck converter topology. A single PWM input signal is all that is required to properly drive the high-side and the low-side MOSFETs. Each part is capable of driving speeds up to 1MHz.

VCIN and Disable (DISB#)

The VCIN pin is monitored by an Under-Voltage Lockout (UVLO) circuit. When V_{CIN} rises above $\sim 3.3V$, the driver is enabled. When V_{CIN} falls below $\sim 2.95V$, the driver is disabled ($GH, GL=0$). The driver can also be disabled by pulling the DISB# pin LOW ($DISB\# < V_{IL_DISB}$), which holds both GL and GH LOW regardless of the PWM input state. The driver can be enabled by raising the DISB# pin voltage HIGH ($DISB\# > V_{IH_DISB}$).

Table 1. UVLO and Disable Logic

UVLO	DISB#	Driver State
0	X	Disabled ($GH, GL=0$)
1	0	Disabled ($GH, GL=0$)
1	1	Enabled (see Table 2)
1	Open	Disabled ($GH, GL=0$)

Note:

- DISB# internal pull-down current source is $10\mu A$.

Thermal Warning Flag (THWN#)

The FDMF3030 provides a thermal warning flag (THWN#) to warn of over-temperature conditions. The thermal warning flag uses an open-drain output that pulls to CGND when the activation temperature ($150^{\circ}C$) is reached. The THWN# output returns to a high-impedance state once the temperature falls to the reset temperature ($135^{\circ}C$). For use, the THWN# output requires a pull-up resistor, which can be connected to VCIN. THWN# does NOT disable the DrMOS module.

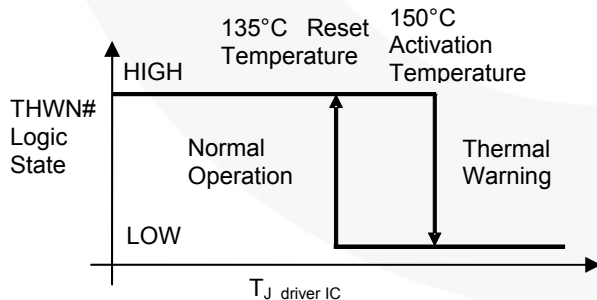


Figure 28. THWN Operation

Three-State PWM Input

The FDMF3030 incorporates a three-state 5V PWM input gate drive design. The three-state gate drive has both logic HIGH level and LOW level, along with a three-state shutdown window. When the PWM input signal enters and remains within the three-state window for a defined hold-off time ($t_{D_HOLD-OFF}$), both GL and GH are pulled LOW. This enables the gate drive to shut down both high-side and low-side MOSFETs to support features such as phase shedding, which is common on multi-phase voltage regulators.

Exiting Three-State Condition

When exiting a valid three-state condition, the FDMF3030 follows the PWM input command. If the PWM input goes from three-state to LOW, the low-side MOSFET is turned on. If the PWM input goes from three-state to HIGH, the high-side MOSFET is turned on. This is illustrated in Figure 29. The FDMF3030 design allows for short propagation delays when exiting the three-state window (see *Electrical Characteristics*).

Low-Side Driver

The low-side driver (GL) is designed to drive a ground-referenced, low- $R_{DS(ON)}$, N-channel MOSFET. The bias for GL is internally connected between the VDRV and CGND pins. When the driver is enabled, the driver's output is 180° out of phase with the PWM input. When the driver is disabled ($DISB\#=0V$), GL is held LOW.

High-Side Driver

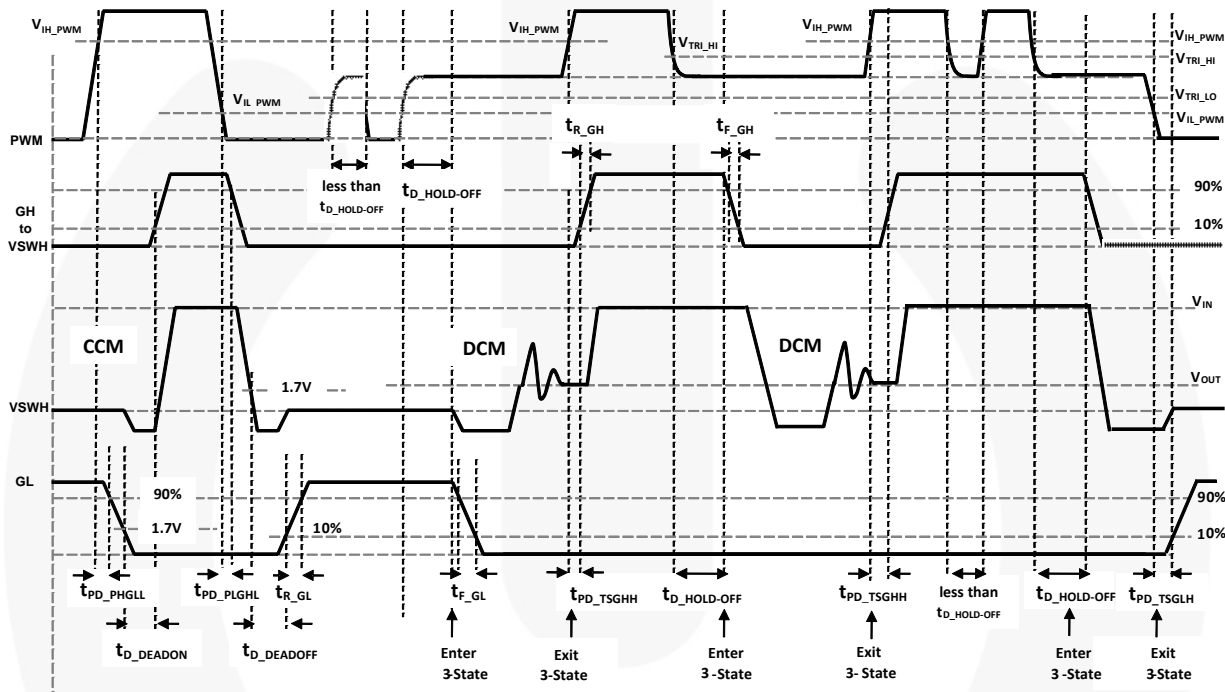
The high-side driver (GH) is designed to drive a floating N-channel MOSFET. The bias voltage for the high-side driver is developed by a bootstrap supply circuit consisting of the internal Schottky diode and external bootstrap capacitor (C_{BOOT}). During startup, V_{SWH} is held at PGND, allowing C_{BOOT} to charge to V_{DRV} through the internal diode. When the PWM input goes HIGH, GH begins to charge the gate of the high-side MOSFET (Q1). During this transition, the charge is removed from C_{BOOT} and delivered to the gate of Q1. As Q1 turns on, V_{SWH} rises to V_{IN} , forcing the BOOT pin to $V_{IN} + V_{BOOT}$, which provides sufficient V_{GS} enhancement for Q1. To complete the switching cycle, Q1 is turned off by pulling GH to V_{SWH} . C_{BOOT} is then recharged to V_{DRV} when V_{SWH} falls to PGND. GH output is in-phase with the PWM input. The high-side gate is held LOW when the driver is disabled or the PWM signal is held within the three-state window for longer than the three-state hold-off time, $t_{D_HOLD-OFF}$.

Adaptive Gate Drive Circuit

The driver IC advanced design ensures minimum MOSFET dead-time, while eliminating potential shoot-through (cross-conduction) currents. It senses the state of the MOSFETs and adjusts the gate drive adaptively to ensure they do not conduct simultaneously. Figure 29 provides the relevant timing waveforms. To prevent overlap during the LOW-to-HIGH switching transition (Q2 off to Q1 on), the adaptive circuitry monitors the voltage at the GL pin. When the PWM signal goes

HIGH, Q2 begins to turn off after a propagation delay (t_{PD_PHGLL}). Once the GL pin is discharged below 1.7V, Q1 begins to turn on after adaptive delay t_{D_DEADON} .

To prevent overlap during the HIGH-to-LOW transition (Q1 off to Q2 on), the adaptive circuitry monitors the voltage at the GH-to-PHASE pin pair. When the PWM signal goes LOW, Q1 begins to turn off after a propagation delay (t_{PD_PLGHL}). Once the voltage across GH-to-PHASE falls below 1.7V, Q2 begins to turn on after adaptive delay $t_{D_DEADOFF}$.



Notes:

t_{PD_xxx} = propagation delay from external signal (PWM, ZCD_EN#, etc.) to IC generated signal. Example (t_{PD_PHGLL} – PWM going HIGH to LS V_{GS} (GL) going LOW)
 t_{D_xxx} = delay from IC generated signal to IC generated signal. Example (t_{D_DEADON} – LS V_{GS} (GL) LOW to HS V_{GS} (GH) HIGH)

PWM

t_{PD_PHGLL} = PWM rise to LS V_{GS} fall, V_{IH_PWM} to 90% LS V_{GS}
 t_{PD_PLGHL} = PWM fall to HS V_{GS} fall, V_{IL_PWM} to 90% HS V_{GS}
 t_{PD_PHGHH} = PWM rise to HS V_{GS} rise, V_{IH_PWM} to 10% HS V_{GS} (ZCD_EN# held LOW)

Exiting 3-state

t_{PD_TSGHH} = PWM 3-state to HIGH to HS V_{GS} rise, V_{IH_PWM} to 10% HS V_{GS}
 t_{PD_TSGHL} = PWM 3-state to LOW to LS V_{GS} rise, V_{IL_PWM} to 10% LS V_{GS}

ZCD_EN#

t_{PD_ZLGL} = ZCD_EN# fall to LS V_{GS} fall, V_{IL_ZCD_EN} to 90% LS V_{GS}
 t_{PD_ZHGLH} = ZCD_EN# rise to LS V_{GS} rise, V_{IH_ZCD_EN} to 10% LS V_{GS}

Dead Times

t_{D_DEADON} = LS V_{GS} fall to HS V_{GS} rise, LS-comp trip value (~1.7V GL) to 10% HS V_{GS}
 $t_{D_DEADOFF}$ = VSWH fall to LS V_{GS} rise, SW-comp trip value (~1.7V VSWH) to 10% LS V_{GS}

Figure 29. PWM and 3-State Timing Diagram

Zero Cross Detection Mode (ZCD_EN#)

The Zero Cross Detection Mode allows for higher converter efficiency when operating in light-load conditions. When ZCD_EN# is pulled LOW; the low-side MOSFET gate signal pulls LOW when internal circuitry detects positive LS MOSFET drain current, preventing discharge of the output capacitors as the filter inductor current attempts reverse current flow – known as “Diode Emulation” Mode.

When the ZCD_EN# pin is pulled HIGH, the synchronous buck converter works in Synchronous Mode, which allows for gating of the low-side MOSFET.

When the ZCD_EN# pin is pulled LOW, the low-side MOSFET is gated off automatically during positive LS MOSFET drain current. If the ZCD_EN# pin is pulled LOW by the PWM controller to support light-load Power-Saving Mode, FDMF3030 can actively turn off the low-side MOSFET when it detects the zero crossing of the inductor current. The low-side MOSFET turns on when inductor current is positive (LS MOSFET drain current is negative) and turns off when inductor current is negative (LS MOSFET drain current is positive). Zero-crossing detection of the inductor current and low-side MOSFET on and off are automatically performed on a cycle-by-cycle basis. Normally this pin is active LOW. See Figure 30 for timing delays.

Table 2. ZCD_EN# Logic

DISB#	PWM	ZCD_EN#	GH	GL
0	X	X	0	0
1	3-State	X	0	0
1	0	0	0	0 ($I_L < 0$), 1 ($I_L > 0$) ⁽⁴⁾
1	1	0	1	0
1	0	1	0	1
1	1	1	1	0

Note:

- GL = 0, when $I_L < 0$ (Inductor current is negative and flowing in to the DrMOS VSWH node). GL = 1 when $I_L > 0$ (Inductor current is positive and flowing out of the DrMOS VSWH node).

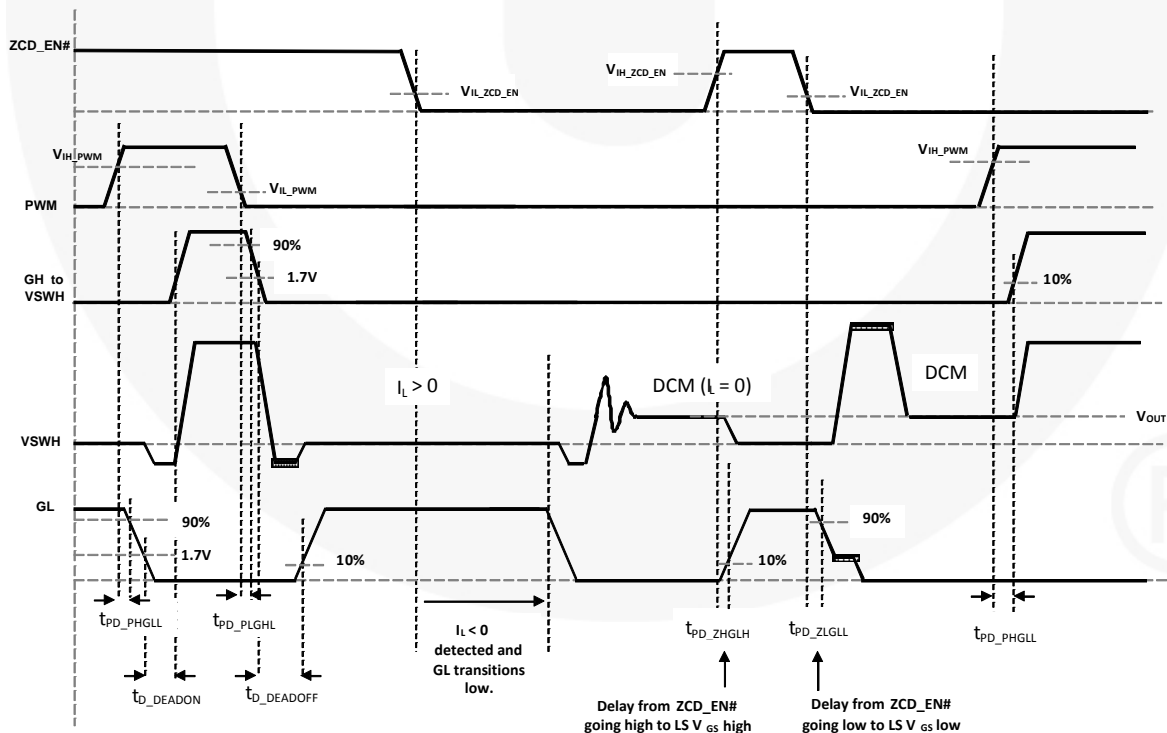


Figure 30. ZCD_EN# Timing Diagram

Application Information

Supply Capacitor Selection

For the supply inputs (V_{CIN}), a local ceramic bypass capacitor is recommended to reduce noise and to supply the peak current. Use at least a $1\mu\text{F}$ X7R or X5R capacitor. Keep this capacitor close to the V_{CIN} pin and connect it to the GND plane with vias.

Bootstrap Circuit

The bootstrap circuit uses a charge storage capacitor (C_{BOOT}), as shown in Figure 31. A bootstrap capacitance of 100nF X7R or X5R capacitor is usually adequate. A series bootstrap resistor may be needed for specific applications to improve switching noise immunity. The boot resistor may be required when operating above $15V_{IN}$ and is effective at controlling the high-side MOSFET turn-on slew rate and V_{SWH} overshoot. R_{BOOT} values from 0.5Ω to 3.0Ω are typically effective in reducing V_{SWH} overshoot.

VCIN Filter

The V_{DRV} pin provides power to the gate drive of the high-side and low-side power MOSFET. In most cases, it can be connected directly to V_{CIN} , the pin that provides power to the logic section of the driver. For additional noise immunity, an RC filter can be inserted between the V_{DRV} and V_{CIN} pins. Recommended values would be 10Ω and $1\mu\text{F}$.

Power Loss and Efficiency

Measurement and Calculation

Refer to Figure 31 for power loss testing method.

Power loss calculations are:

$$P_{IN} = (V_{IN} \times I_{IN}) + (V_{5V} \times I_{5V}) \text{ (W)} \quad (1)$$

$$P_{SW} = V_{SW} \times I_{OUT} \text{ (W)} \quad (2)$$

$$P_{OUT} = V_{OUT} \times I_{OUT} \text{ (W)} \quad (3)$$

$$P_{LOSS_MODULE} = P_{IN} - P_{SW} \text{ (W)} \quad (4)$$

$$P_{LOSS_BOARD} = P_{IN} - P_{OUT} \text{ (W)} \quad (5)$$

$$EFFI_{MODULE} = 100 \times P_{SW}/P_{IN} \text{ (\%)} \quad (6)$$

$$EFFI_{BOARD} = 100 \times P_{OUT}/P_{IN} \text{ (\%)} \quad (7)$$

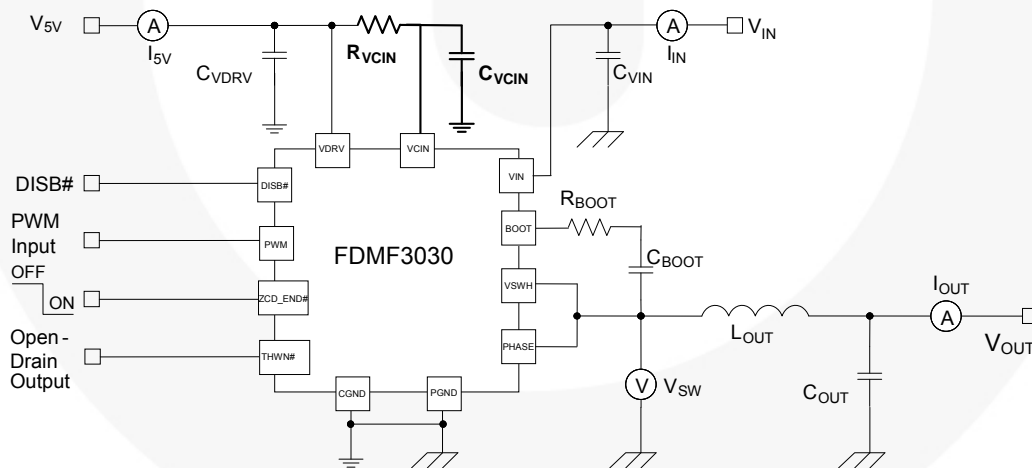


Figure 31. Circuit Diagram and Power Loss Measurement

PCB Layout Guidelines

Figure 32 and Figure 33 provide an example of a proper layout for the FDMF3030 and critical components. All of the high-current paths; such as VIN, VSWH, VOUT, and GND copper; should be short and wide for low inductance and resistance. This aids in achieving a more stable and evenly distributed current flow, along with enhanced heat radiation and system performance.

Recommendations for PCB Designers

Input ceramic bypass capacitors must be placed close to the VIN and PGND pins. This reduces the high-current power loop inductance and the input current ripple induced by power MOSFET switching operation.

The V_{SWH} copper trace serves two purposes. In addition to being the high-frequency current path from the DrMOS package to the output inductor, it serves as a heat sink for the low-side MOSFET in the DrMOS package. The trace should be short and wide enough to present a low-impedance path for the high-frequency, high-current flow between the DrMOS and inductor. The short and wide trace minimizes electrical losses as well as the DrMOS temperature rise. The V_{SWH} node is a high-voltage and high-frequency switching node with high noise potential. Care should be taken to minimize coupling to adjacent traces. Since this copper trace acts as a heat sink for the lower MOSFET, balance using the largest area possible to improve DrMOS cooling while maintaining acceptable noise emission.

An output inductor should be located close to the FDMF3030 to minimize the power loss due to the V_{SWH} copper trace. Care should also be taken so the inductor dissipation does not heat the DrMOS.

PowerTrench[®] MOSFETs are used in the output stage and minimize ringing due to fast switching. In most cases, no VSWH snubber is required. If a snubber is used, it should be placed close to the VSWH and PGND pins. The selected resistor and capacitor need to be the proper size for power dissipation.

VCIN, VDRV, and BOOT capacitors should be placed as close as possible to the VCIN-to-CGND, VDRV-to-CGND, and BOOT-to-PHASE pin pairs to ensure clean and stable power. Routing width and length should be considered as well.

Include a trace from the PHASE pin to the VSWH pin to improve noise margin. Keep this trace as short as possible.

The layout should include the option to insert a small-value series boot resistor between the boot capacitor and BOOT pin. The boot-loop size, including R_{BOOT} and C_{BOOT}, should be as small as possible. The boot resistor

may be required when operating above 15V_{IN} and is effective at controlling the high-side MOSFET turn-on slew rate and V_{SHW} overshoot. R_{BOOT} can improve noise operating margin in synchronous buck designs that may have noise issues due to ground bounce or high positive and negative V_{SWH} ringing. Inserting a boot resistance lowers the DrMOS efficiency. Efficiency versus noise trade-offs must be considered. R_{BOOT} values from 0.5Ω to 3.0Ω are typically effective in reducing V_{SWH} overshoot.

The VIN and PGND pins handle large current transients with frequency components greater than 100MHz. If possible, these pins should be connected directly to the VIN and board GND planes. The use of thermal relief traces in series with these pins is discouraged since this adds inductance to the power path. This added inductance in series with either the VIN or PGND pin degrades system noise immunity by increasing positive and negative V_{SWH} ringing.

GND pad and PGND pins should be connected to the GND copper plane with multiple vias for stable grounding. Poor grounding can create a noise transient offset voltage level between CGND and PGND. This could lead to faulty operation of the gate driver and MOSFETs and should be avoided.

Ringing at the BOOT pin is most effectively controlled by close placement of the boot capacitor. Do not add an additional BOOT to the PGND capacitor. This may lead to excess current flow through the BOOT diode.

The ZCD_EN# and DISB# pins have weak internal pull-up and pull-down current sources, respectively. These pins should not have any noise filter capacitors. Do not float these pins unless absolutely necessary.

Use multiple vias on the VIN and VOUT copper areas to interconnect top, inner, and bottom layers to distribute current flow and heat conduction. Do not put many vias on the VSWH copper to avoid extra parasitic inductance and noise on the switching waveform. As long as efficiency and thermal performance are acceptable, place only one VSWH copper on the top layer and use no vias on the VSWH copper to minimize switch node parasitic noise. Vias should be relatively large and of reasonably low inductance. Critical high-frequency components, such as R_{BOOT}, C_{BOOT}, RC snubber, and bypass capacitors; should be located as close to the respective DrMOS module pins as possible on the top layer of the PCB. If this is not feasible, they can be connected from the backside through a network of low-inductance vias.

PCB Layout Guidelines (Continued)

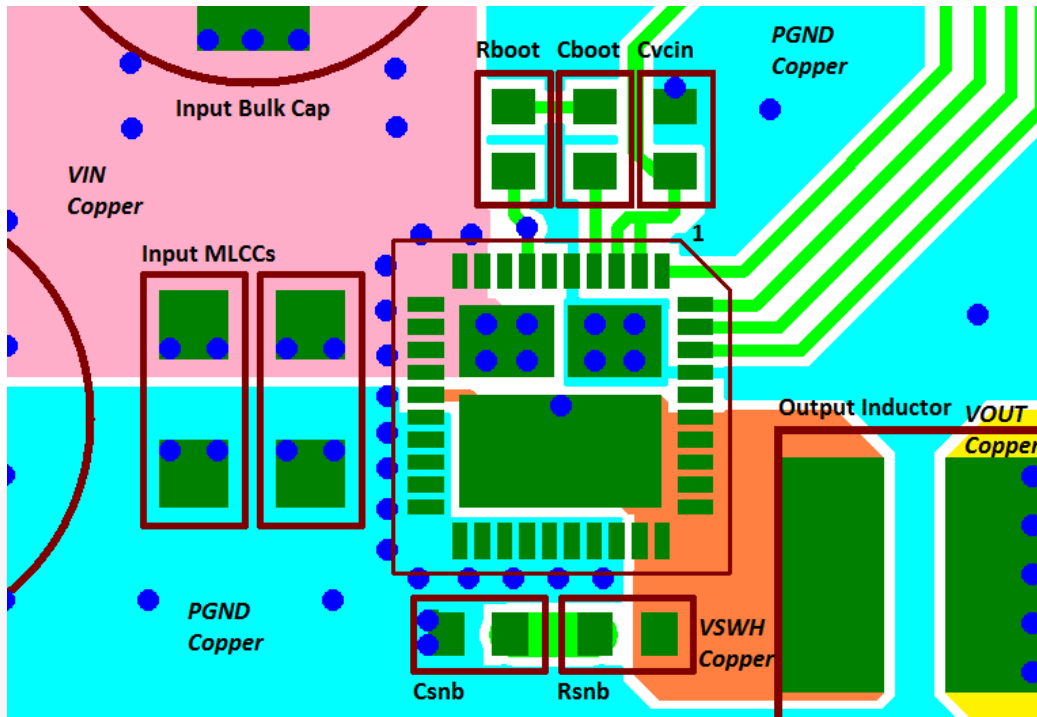


Figure 32. PCB Layout Example (Top View)

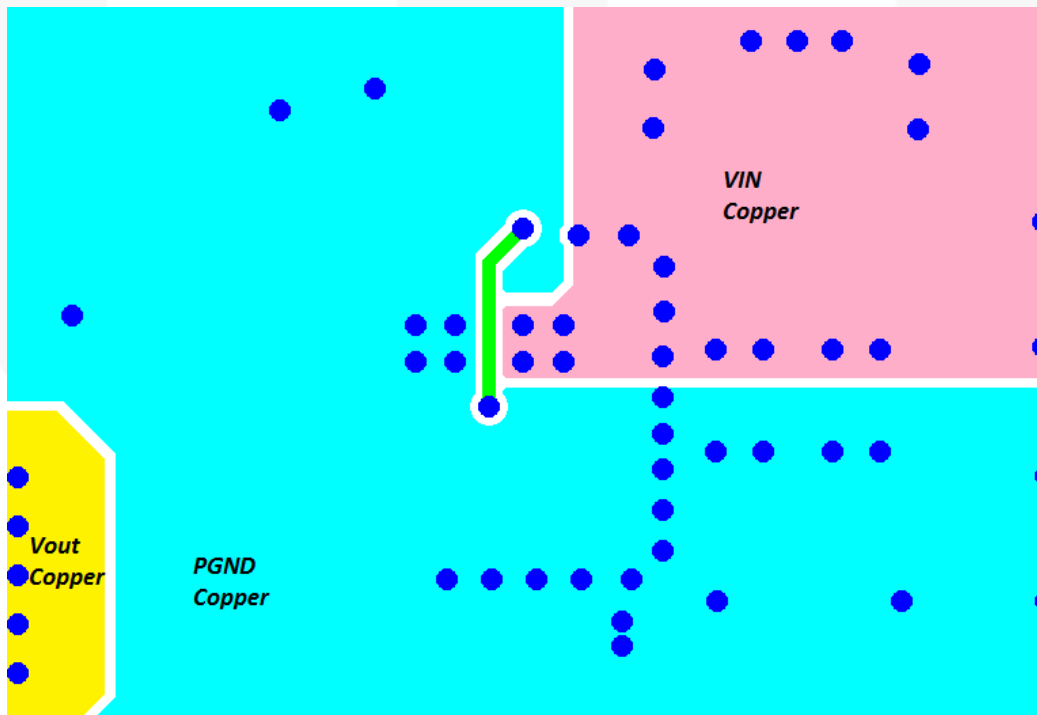


Figure 33. PCB Layout Example (Bottom View)

Physical Dimensions

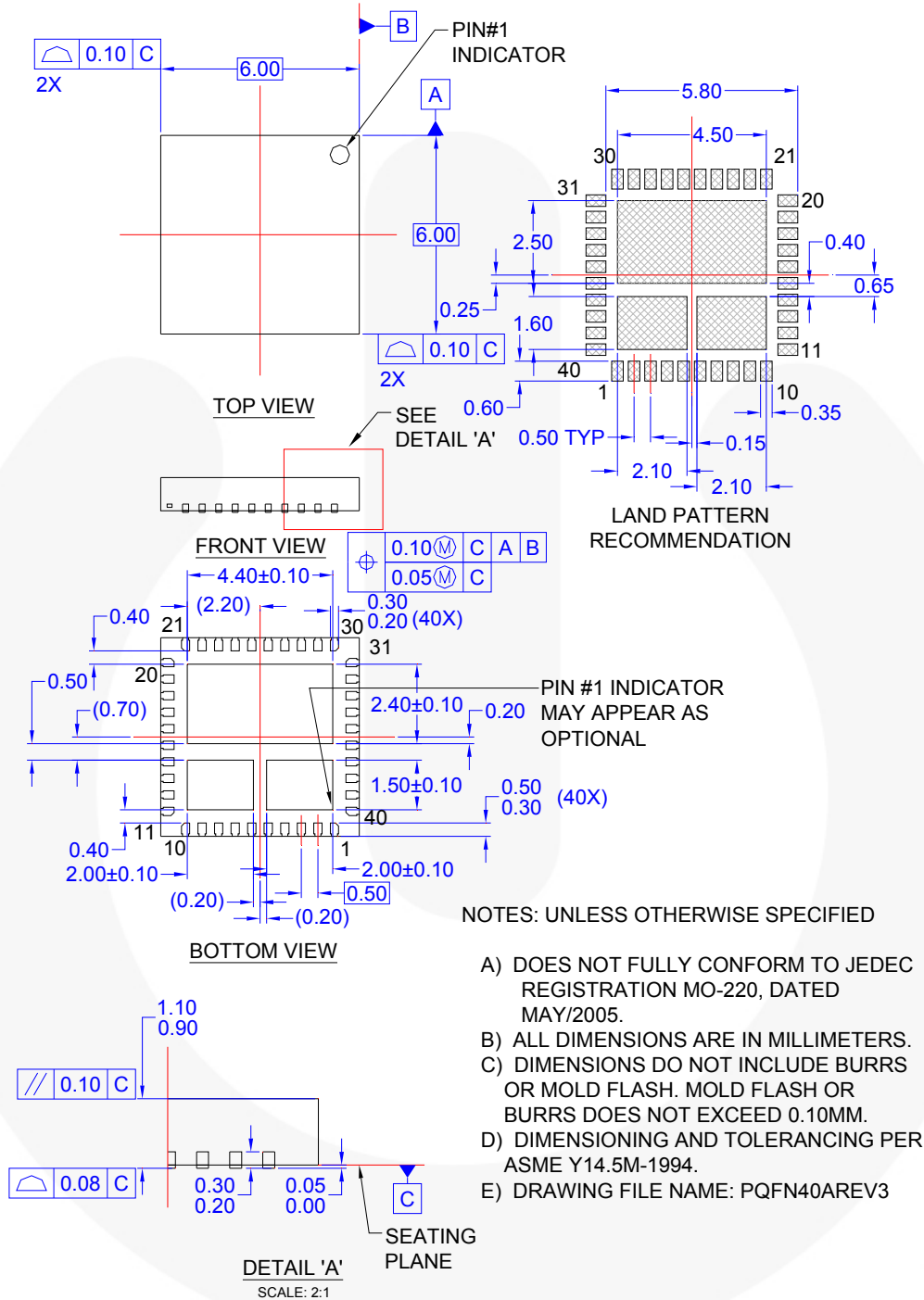


Figure 34. 40-Lead, Clipbond PQFN DrMOS, 6.0x6.0mm Package





Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:
<http://www.fairchildsemi.com/packaging/>



TRADEMARKS

The following includes registered and unregistered trademarks and service marks, owned by Fairchild Semiconductor and/or its global subsidiaries, and is not intended to be an exhaustive list of all such trademarks.

- | | | | |
|--|--|---|---|
| 2Cool™ | F-PFS™ | PowerTrench® | The Power Franchise® |
| AccuPower™ | FRFET® | PowerXS™ | the power franchise |
| AX-CAP™* | Global Power Resource SM | Programmable Active Droop™ | TinyBoost™ |
| BitSiC™ | GreenBridge™ | QFET® | TinyBuck™ |
| Build it Now™ | Green FPS™ | QS™ | TinyCalc™ |
| CorePLUS™ | Green FPS™ e-Series™ | Quiet Series™ | TinyLogic® |
| CorePOWER™ | Gmax™ | RapidConfigure™ | TINYOPTO™ |
| CROSSVOLT™ | GTO™ |  | TinyPower™ |
| CTL™ | IntelliMAX™ | Saving our world, 1mW/W/kW at a time™ | TinyPWM™ |
| Current Transfer Logic™ | ISOPLANAR™ | SignalWise™ | TinyWire™ |
| DEUXPEED® | Making Small Speakers Sound Louder and Better™ | SmartMax™ | TranSiC™ |
| Dual Cool™ | MegaBuck™ | SMART START™ | TriFault Detect™ |
| EcoSPARK® | MICROCOUPLER™ | Solutions for Your Success™ | TRUECURRENT®* |
| EfficientMax™ | MicroFET™ | SPM® | µSerDes™ |
| ESBC™ | MicroPak™ | STEALTH™ |  |
|  Fairchild® | MicroPak2™ | SuperFET® | UHC® |
| Fairchild Semiconductor® | MillerDrive™ | SuperSOT™-3 | Ultra FRFET™ |
| FACT Quiet Series™ | MotionMax™ | SuperSOT™-6 | UniFET™ |
| FACT® | mWSaver™ | SuperSOT™-8 | VCX™ |
| FAST® | OptoHiT™ | SupreMOS® | VisualMax™ |
| FastvCore™ | OPTOLOGIC® | SyncFET™ | VoltagePlus™ |
| FETBench™ | OPTOPLANAR® | Sync-Lock™ | XS™ |
| FlashWriter®* | |  | |
| FPS™ | | | |

* Trademarks of System General Corporation, used under license by Fairchild Semiconductor.

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

ANTI-COUNTERFEITING POLICY

Fairchild Semiconductor Corporation's Anti-Counterfeiting Policy. Fairchild's Anti-Counterfeiting Policy is also stated on our external website, www.fairchildsemi.com, under Sales Support.

Counterfeiting of semiconductor parts is a growing problem in the industry. All manufacturers of semiconductor products are experiencing counterfeiting of their parts. Customers who inadvertently purchase counterfeit parts experience many problems such as loss of brand reputation, substandard performance, failed applications, and increased cost of production and manufacturing delays. Fairchild is taking strong measures to protect ourselves and our customers from the proliferation of counterfeit parts. Fairchild strongly encourages customers to purchase Fairchild parts either directly from Fairchild or from Authorized Fairchild Distributors who are listed by country on our web page cited above. Products customers buy either from Fairchild directly or from Authorized Fairchild Distributors are genuine parts, have full traceability, meet Fairchild's quality standards for handling and storage and provide access to Fairchild's full range of up-to-date technical and product information. Fairchild and our Authorized Distributors will stand behind all warranties and will appropriately address any warranty issues that may arise. Fairchild will not provide any warranty coverage or other assistance for parts bought from Unauthorized Sources. Fairchild is committed to combat this global problem and encourage our customers to do their part in stopping this practice by buying direct or from authorized distributors.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

Rev. I62

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5817-1050

ON Semiconductor Website: www.onsemi.com
Order Literature: <http://www.onsemi.com/orderlit>
For additional information, please contact your local
Sales Representative