NB7VPQ701M

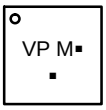
1.8 V USB 3.1 Single Channel Re-driver

ON Semiconductor®

www.onsemi.com

UQFN12
CASE 523AV

MARKING DIAGRAM



VP = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

Description

The NB7VPQ701M is a 1.8 V single channel re−driver for USB 3.1 Gen 1 and USB 3.1 Gen 2 applications that supports both 5 Gbps and 10 Gbps data rates. Signal integrity degrades from PCB traces, transmission cables, and inter−symbol interference (ISI). The NB7VPQ701M compensates for these losses by engaging varying levels of equalization at the input receiver and de−emphasis on output driver. The output transmitter circuitry provides user selectable de−emphasis and output amplitude settings to create the best eye openings for the outgoing data signals.

The NB7VPQ701M features an intelligent LFPS circuit. This circuit senses the low frequency signals and automatically disables driver de−emphasis for full USB 3.1 Gen 1 and USB 3.1 Gen 2 compliances.

After power up, the NB7VPQ701M periodically checks both of the TX output pairs for a receiver connection. When the receiver is detected the RX termination becomes enabled and the NB7VPQ701M is set to perform the re−driver function.

The NB7VPQ701M comes in a small, ultra−thin 1.6 x 1.6 mm UQFN12 package and is specified to operate across the entire industrial temperature range, –40°C to 85°C.

Features

- 1.8 V ± 5% Power Supply
- Device Supports USB 3.1 Gen 1 and USB 3.1 Gen 2 Data Rates
- Automatic LFPS De−Emphasis Control
- Automatic Receiver Termination Detection
- Integrated Input and Output Termination
- Selectable Equalization, De−Emphasis, and Output Swing
- Chip Enable Pin for Deep Power−Saving Mode
- Hot−Plug Capable
- ESD Protection ±4 kV HBM
- Operating Temperature Range: –40°C to 85°C
- Small 1.6 x 1.6 x 0.5 mm UQFN12 Package
- This is a Pb−Free Device

Typical Applications

- Mobile Phone and Tablet
- Computer and Laptop
- Docking Station and Dongle
- Active Cable, Back Planes
- Gaming Console, Smart T.V.

ORDERING INFORMATION

Device	Package	Shipping†
NB7VPQ701MMUTBG	UQFN12 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

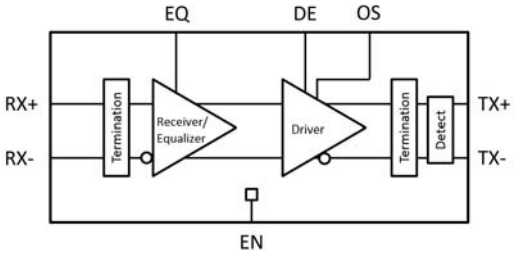


Figure 1. Logic Diagram of NB7VPQ701M

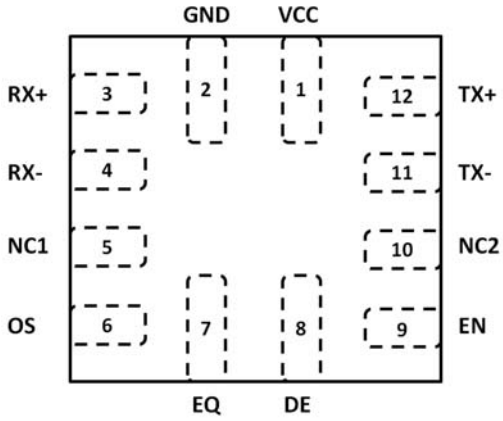


Figure 2. UQFN12 Package Pinout
(Top View)

Table 1. PIN DESCRIPTION

Pin Number	Pin Name	Type	Description
1	VCC	Power	1.8 V power supply
2	GND	Power	Reference Ground
3	RX+	Differential Input Pair	Differential input pair for 5 / 10 Gbps USB signals. Must be externally AC−coupled.
4	RX-		
5	NC1	N/A	No connect – float pin
6	OS	CMOS Input	Sets output amplitude on the TX. 3−state input with integrated 250 kΩ pull−up and pull−down resistors. Defaults to Mid when left open.
7	EQ	CMOS Input	Sets equalizer gain on the RX. 3−state input with integrated 250 kΩ pull−up and pull−down resistors. Defaults to Mid when left open.
8	DE	CMOS Input	Sets the output de−emphasis. 3−state input with integrated 250 kΩ pull−up and pull−down resistors. Defaults to Mid when left open.
9	EN	CMOS Input	Chip enable input (active high), internal 550 kΩ pull−up resistor. Low to power down.
10	NC2	N/A	No connect – float pin
11	TX-	Differential Output Pair	Differential output for 5 / 10 Gbps USB signals. Must be externally AC−coupled.
12	TX+		

DEVICE CONFIGURATION

Table 2. CONTROL PIN EFFECTS (Typical Values)

Pin	Description	Logic State	Equalization Gain		
EQ	Equalization Amount	Low	3 dB		
		Mid	6 dB		
		High	9 dB		
			De−emphasis Ratio (Note 1)		
Pin	**Description**	**Logic State**	**OS = LOW**	**OS = Float**	**OS = High**
DE	De−Emphasis Amount	Low	0 dB	−4 dB	−6 dB
		Mid	−3 dB	−5.5 dB	−7.5 dB
		High	−5.5 dB	−7 dB	−9 dB
Pin	**Description**	**Logic State**	**Output Swing**		
OS	Output Swing with DE Pin Low (0 dB)	Low	750 mV_{PP}		
		Mid	900 mV_{PP}		
		High	1000 mV_{PP}		
Pin	**Description**	**Logic State**	**Chip Enable**		
EN	Chip Enable Input	Low	Chip Disabled (Deep Power−Saving Mode)		
		High	Chip Enable		

1. dB Decrease = 20 log * ($V_{TX−DE}$ / $V_{TX−DIFF−PP}$)

Table 3. ATTRIBUTES

Parameter		
ESD Protection	Human Body Model Charged Device Model	> 4 kV > 1.5 kV
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 2)		Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−O @ 0.125 in
Transistor Count		704
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

2. For additional information, see Application Note AND8003/D.

Table 4. ABSOLUTE MAXIMUM RATINGS

Over operating free−air temperature range (unless otherwise noted)

Parameter	Description	Min	Max	Unit
Supply Voltage (Note 3)	V_{CC}	−0.3	2.5	V
Voltage range at any input or output terminal	Differential I/O	−0.5	1.89	V
	LVCMOS inputs	−0.3	V_{CC} + 0.3	V
Electrostatic discharge	Human body model (all pins) (Note 4)		±4	kV
	Charged device model (all pins) (Note 4)		±1.5	kV
Storage temperature, T_{SG}		−65	150	°C
Maximum junction temperature, T_J		−40	125	°C
Junction−to−ambient thermal resistance, θ_{JA}			138	°C/W

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

3. All voltage values are with respect to the GND terminals.
4. Tested in accordance with JEDEC Standard.

Table 5. RECOMMENDED OPERATING CONDITIONS

Over operating free−air temperature range (unless otherwise noted)

Parameter	Description	Min	Nom	Max	Unit
V_{CC}	Main power supply	1.71	1.8	1.89	V
T_A	Operating free−air temperature	−40		+85	°C
C_{AC}	AC coupling capacitor	75	100	200	nF

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 6. POWER SUPPLY CHARACTERISTICS

Parameter		Test Conditions	Min	Typ (Note 5)	Max	Unit
I_{CC}	Active	Link in U0 with SS data transmission DE = low 0 dB, EQ = low 3 dB, OS = low		65		mA
	Idle State	Link has some activity, not in U0 DE = mid −3 dB, EQ = mid 6dB OS = low		49		mA
	U2/U3	Link in U2 or U3 power saving state DE = mid −3 dB, EQ = mid 6 dB, OS = low		4.5		mA
	No USB Connection	No connection state, termination disabled DE = mid −3 dB, EQ = mid 6 dB, OS = low		4.5		mA
	Deep Power−Saving State	Part disabled by EN pin EN = low		28		μA

5. TYP values use V_{CC} = 1.8 V, T_A = 25°C.

Table 7. LVCMOS CONTROL PIN CHARACTERISTICS

Parameter		Test Conditions	Min	Typ	Max	Unit
3−State LVCMOS Inputs (EQ, DE, OS) and 2−State LVCMOS Inputs (EN)						
V_{IH}	High−level input voltage		0.8 * V_{CC}		V_{CC}	V
V_{IM}	Mid−level input voltage		0.4 * V_{CC}	V_{CC} / 2	0.6 * V_{CC}	V
V_{IL}	Low−level input voltage		GND		0.2 * V_{CC}	V
V_F	Floating voltage	V_{IN} = High impedance		V_{CC} / 2		V
R_{PU}	Internal pull−up resistance			250		kΩ
R_{PD}	Internal pull−down resistance			250		kΩ
I_{IH}	High−level input current	V_{IN} = 1.89 V			20	μA
I_{IL}	Low−level input current	V_{IN} = GND, V_{CC} = 1.89 V	−20			μA

Table 8. RECEIVER AC/DC CHARACTERISTICS Over operating free−air temperature range (unless otherwise noted)

Parameter		Test Conditions	Min	Typ	Max	Unit
VRX−DIFF−pp	Input differential voltage swing	AC−coupled, peak−to−peak	250		1200	mV_{PP}
VRX−CM	Common−mode voltage bias in the receiver (DC)			V_{CC}− 0.25		V
ZRX−DIFF	Differential input impedance (DC)	Present after an USB device is detected on TX+/TX−	80	100	120	Ω
ZRX−CM	Common−mode input impedance (DC)	Present after an USB device is detected on TX+/TX−	20	25	30	Ω
ZRX−HIGH−IMP	Common−mode input impedance with termination disabled (DC)	Present when no USB device is detected on TX+	25	35		kΩ
VTH−LFPS−pp	Low Frequency Periodic Signaling (LFPS) Detect Threshold	Output voltage is considered squelched below this threshold voltage.			300	mV_{PP}

Table 9. TRANSMITTER AC/DC CHARACTERISTICS Over operating free−air temperature range (unless otherwise noted)

Parameter		Test Conditions	Min	Typ	Max	Unit
VTX−DIFF−PP	Output differential voltage swing at 5 Gbps, 10 Gbps with DE low (0 dB)	OS = Low, 50 Ω to V_{CC}		750		mV_{PP}
		OS = Mid, 50 Ω to V_{CC}		900		
		OS = High, 50 Ω to V_{CC}		1000		
CTX	TX input capacitance to GND	At 2.5 GHz		1.25		pF
ZTX−DIFF	Differential output impedance (DC)	Present after an USB device is detected on TX+/TX−	80	100	120	Ω
ZTX−CM	Common−mode output impedance (DC)	Present after an USB device is detected on TX+/TX−	20		30	Ω
ITX−SC	TX short circuit current	TX+ or TX− shorted to GND		30		mA
VTX−CM	Common−mode voltage bias in the transmitter (DC)			V_{CC}−0.5	V_{CC}	V
VTX−CM−ACpp	AC common−mode peak−to−peak voltage swing in active mode	Within U0 and within LFPS			100	mV_{PP}
VTX−IDLE−DIFF−ACpp	Differential voltage swing during electrical idle	Tested with a high−pass filter	0		10	mV_{PP}
VTX−RXDET	Voltage change to allow receiver detect	Positive voltage to sense receiver termination			600	mV
t_R, t_F	Output rise, fall time	20% − 80% of differential voltage measured 1 inch from the output pin		45		ps
t_{RF-MM}	Output rise, Fall time mismatch	20% − 80% of differential voltage measured 1 inch from the output pin			5	ps
$t_{diff-LH}$, $t_{diff-HL}$	Differential propagation delay	De−emphasis = −3 dB, OS = Low propagation delay between 50% level at input and output		150		ps
$t_{idleEntry}$, $t_{idleExit}$	Idle entry and exit times			30		ns

Table 10. TIMING AND JITTER CHARACTERISTICS

Parameter		Test Conditions	Min	Typ	Max	Unit
TIMING						
tREADY	Time from power applied until RX termination is enabled	Apply 0 V to V_{CC}, connect USB termination to TX±, apply 1.8 V to V_{CC}, and measure when ZRX−DIFF is enabled		10		ms
JITTER FOR 5 Gbps						
TJTX−EYE	Total jitter (Notes 6, 7)	EQ = Mid 6 dB, DE = High −5.5 dB, OS = Low		0.087		UI (Note 8)
DJTX	Deterministic jitter (Note 7)			0.023		UI (Note 8)
RJTX	Random jitter (Note 7)			0.006		UI (Note 8)
JITTER FOR 10 Gbps						
TJTX−EYE	Total jitter (Notes 6, 7)	EQ = Mid 6dB, DE = High −5.5 dB, OS = Low		0.207		UI (Note 8)
DJTX	Deterministic jitter (Note 7)			0.082		UI (Note 8)
RJTX	Random jitter (Note 7)			0.013		UI (Note 8)

6. Includes RJ at 10^{-12}.
7. Measured at the ends of reference channel with a K28.5 pattern, VID = 1000 mVpp, −3.5 dB de−emphasis from source.
8. 5 Gbps, UI = 200 ps for 10 Gbps, UI = 100 ps

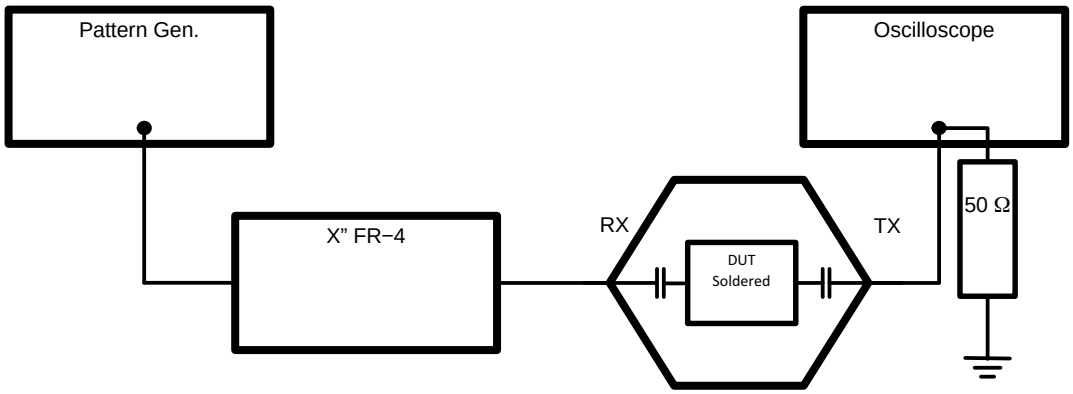


Figure 3. Equalization Measurement Setup

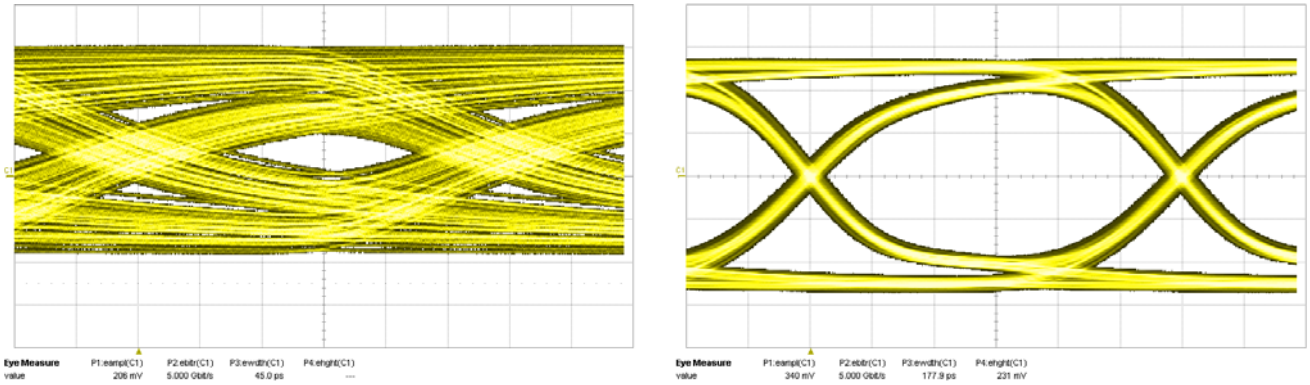


Figure 4. 5 Gbps Signal with 24 inches of FR4 Before Input to NB7VPQ701M and After Using High EQ Setting

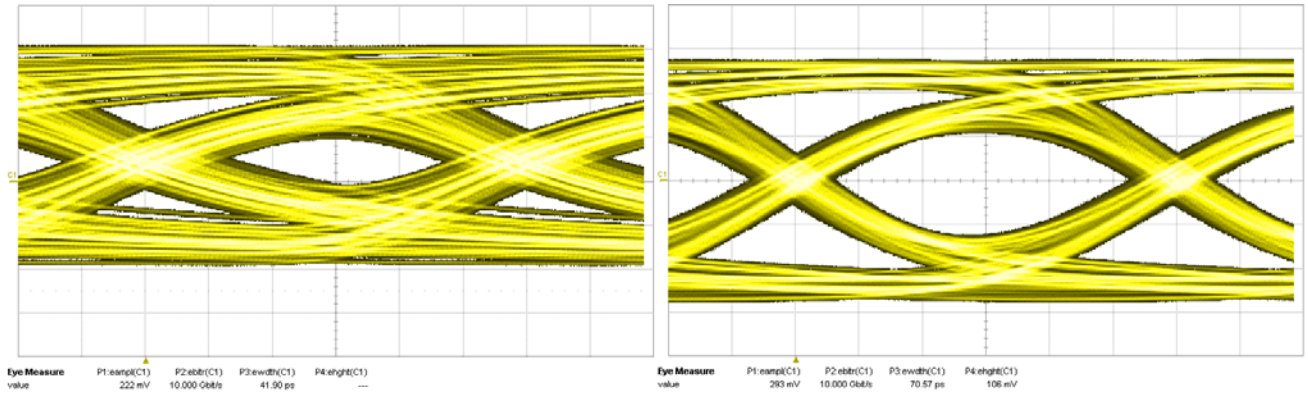


Figure 5. 10 Gbps Signal with 12 inches of FR4 Before Input to NB7VPQ701M and After with EQ Floating (Mid)

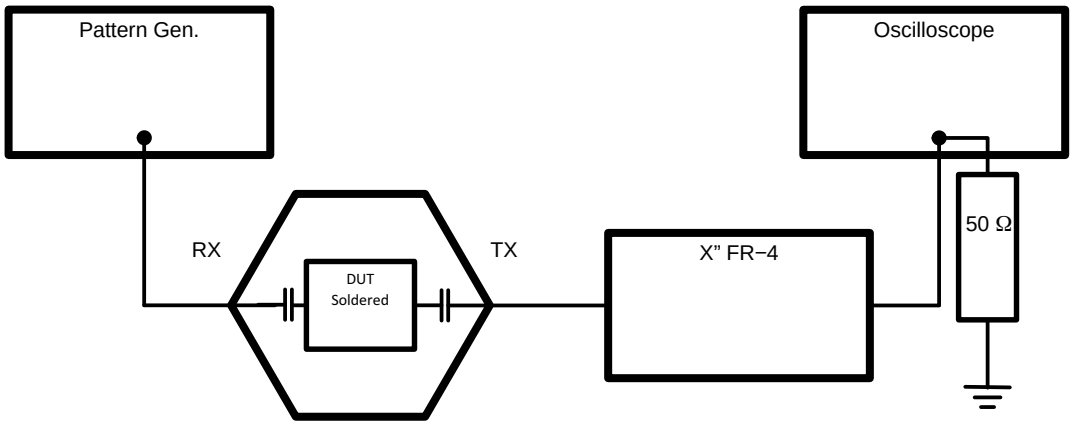


Figure 6. De−Emphasis Measurement Setup

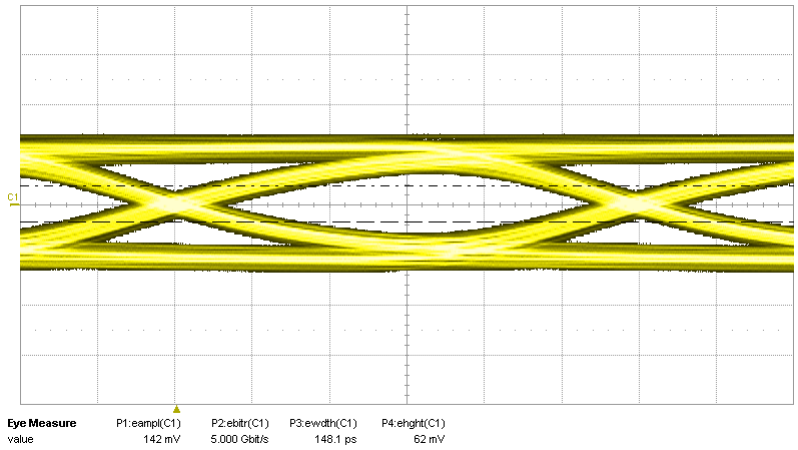


Figure 7. 5 Gbps Signal After 24 inches of FR4 at Output with High DE Setting to NB7VPQ701M

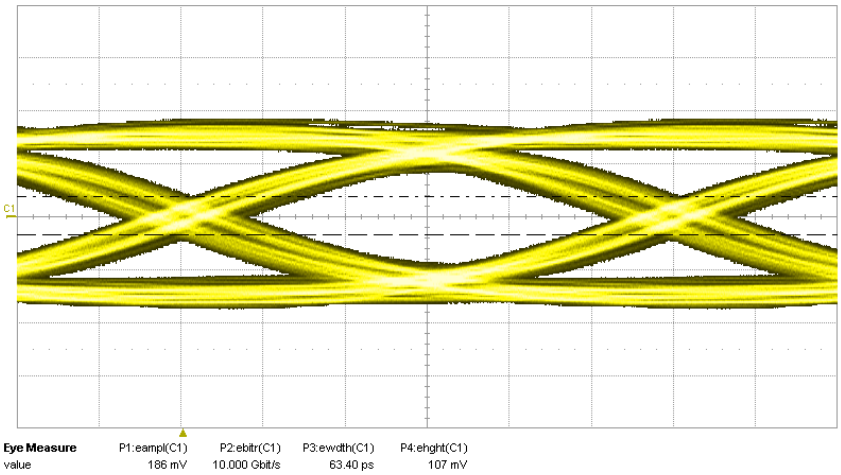


Figure 8. 10 Gbps Signal After 9 inches of FR4 at Output with High DE Setting to NB7VPQ701M

PARAMETER MEASUREMENT DIAGRAMS

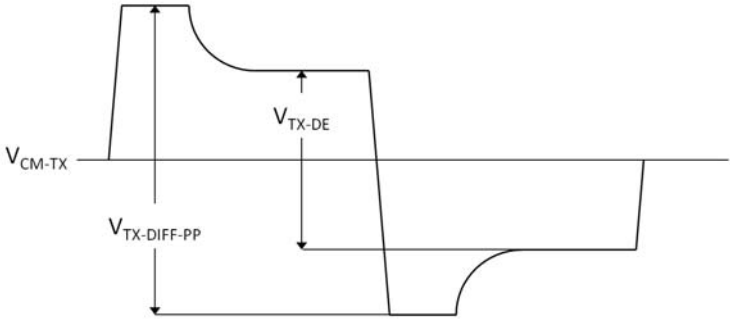


Figure 9. Transmitter Differential Voltage
dB Decrease = 20 log * (V_{TX-DE} / $V_{TX-DIFF-PP}$)

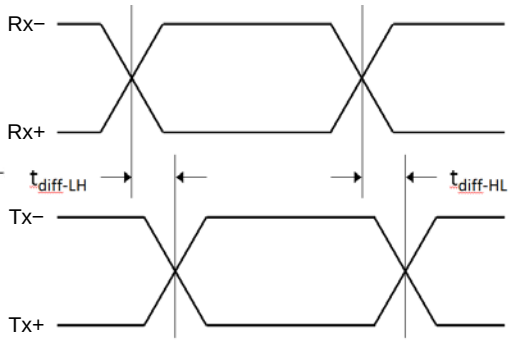


Figure 10. Propagation Delay

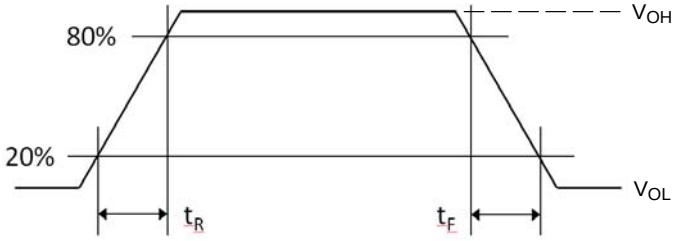


Figure 11. Output Rise and Fall Times

APPLICATION GUIDELINES

LFPS Compliance Testing

As part of USB 3.1 compliance test, the host or peripheral must transmit a LFPS signal that adheres to the spec parameters. When using a real−time oscilloscope to capture this data, *the scope's trigger must be below 0 V when making single−ended measurements*. Although the differential signal is identical to that which is expected by the USB 3.1 system, the AC common mode voltage for LFPS may fall below 0 V during short bursts of switching signal, which is still within the spec's limit.

LFPS Functionality

USB 3.1 links use Low Frequency Periodic Signaling (LFPS) to implement functions like exiting low−power modes, performing warm resets and providing link training between host and peripheral devices. LFPS signaling consists of bursts of frequencies ranging between 10 to 50 MHz and can have specific burst lengths or repeat rates.

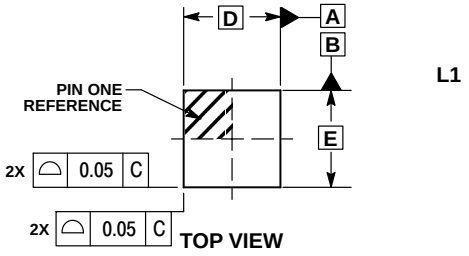
Ping.LFPS for TX Compliance

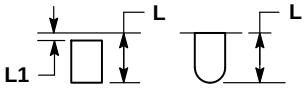
During the transmitter compliance, the system under test must transmit certain compliance patterns as defined by the USB−IF. In order to toggle through these patterns for various tests, the receiver must receive a ping. LFPS signal from either the test suite or a separate pattern generator. The standard signal comprises of a single burst period of 100ns at 20 MHz. In order to pass this signal through NB7VPQ701M, *the duration of the burst must be extended to at least 200 ns.*

NB7VPQ701M

PACKAGE DIMENSIONS

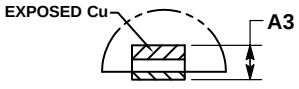
UQFN12, 1.6x1.6, 0.4P
CASE 523AV
ISSUE A

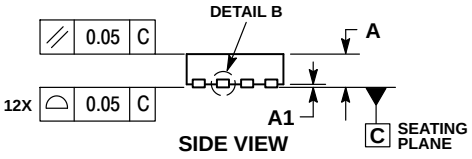


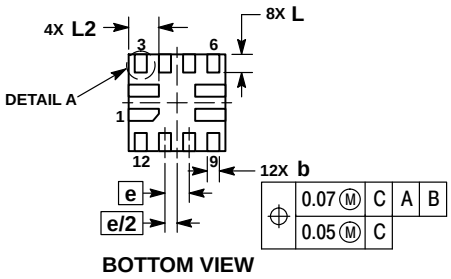


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.25 mm FROM THE TERMINAL TIP.

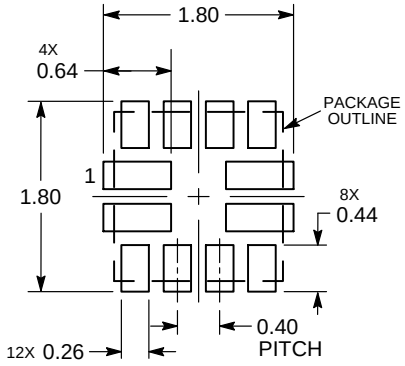
	MILLIMETERS	
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.152 REF	
b	0.15	0.25
D	1.60 BSC	
E	1.60 BSC	
e	0.40 BSC	
L	0.20	0.40
L2	0.40	0.60







SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

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