MLX90292

SMD Programmable Linear Hall Sensor IC
PWM / PAS4 / PSI5-A

Features and Benefits

- Programmable Hall effect sensor
  - 12-bit magnetic flux density
  - 8-bit temperature (PAS4 & PSI-5)
  - Extensive diagnostic
  - Embedded µ-controller
  - Piecewise linearization
- Dual die for redundancy (safety)
- Measurement range from ±30mT to ±170mT
- Programmable through the connector
- Dual customer area for supply chain split
- Over 48 bit customer IDs available
- TSSOP16 SMD package RoHS compliant
- Lead free component, suitable for lead free soldering profile 260°C

Application Examples

- Rotary position sensor
- Linear position sensor

Ordering Code

Product Code	Temperature Code	Package Code	Option Code	Packing Form Code
MLX90292	L	GO	CAE-000	RE
MLX90292	L	GO	CAE-000	TU

Legend:

Temperature Code:	L for Temperature Range -40°C to 150°C
Package Code:	GO for TSSOP16
Option Code:	xxx-000: Standard version
Packing Form:	RE for Reel
	TU for Tube
Ordering example:	MLX90292LGO-CAE-000-RE

1. Functional Diagram

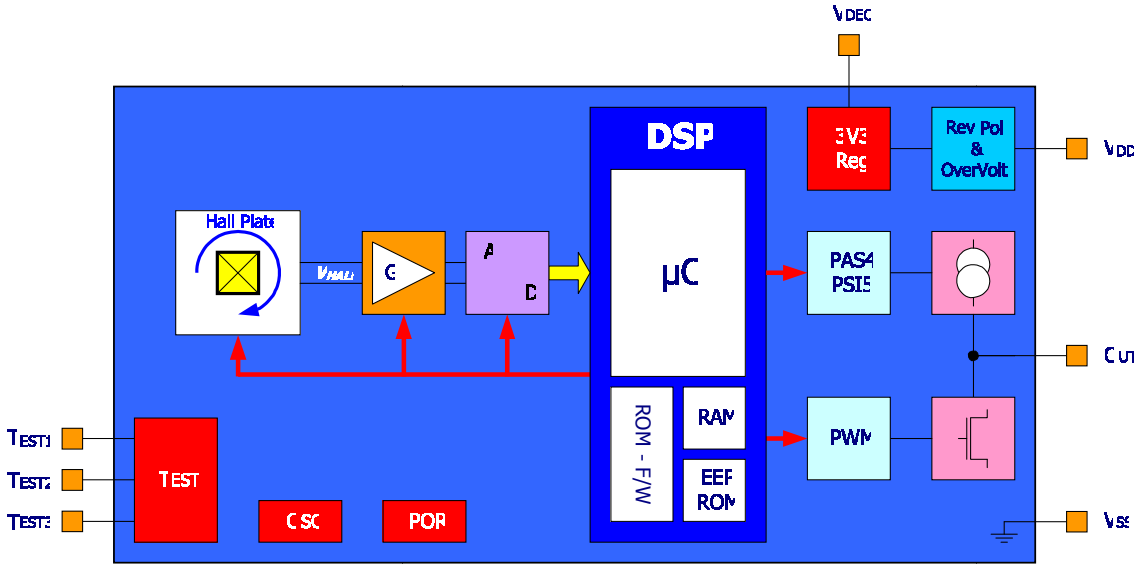

Figure 1: Functional Block Diagram

2. Description

The MLX90292 is a CMOS Hall sensor with embedded µController. With its specific architecture and the help of a dedicated firmware, the magnetic flux density perpendicular to the chip surface can be measured. It is designed for contact-less magnetic flux measurement that is frequently required in automotive electrical power steering applications.

The MLX90292 is a dual die and the following specification is valid for both die.

The front-end part of the sensor measures the perpendicular magnetic field and converts it into digital data. This data is pre-calibrated (offset, sensitivity matching, temperature correction) and is then transmitted over a digital interface to the electronic control unit (ECU).

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3. Glossary of Terms

Gauss (G), Tesla (T): Magnetic flux density units where 1 mT = 10 G.
ADC: Analog-to-Digital Converter
ASP: Analog Signal Processing
DSP: Digital Signal Processing
EEPROM: Electrically Erasable Programmable Read Only Memory
ESD: Electro-Static Discharge
µC: Micro-controller
MUX: Multiplexer
OSC: Oscillator
RAM: Random Access Memory
TC: Sensitivity Temperature Coefficient (in ppm/Deg.C.).
POR: Power On Reset
PSI: Peripheral Sensor Interface
PAS: Peripheral Acceleration Interface
S/W: Firmware
H/W: Hardware

4. Pin description

The MLX90292 is available as a 16-pin dual die package, with the following pinout.

Pin #	Name	I/O	Description	Die 1	Die 2
1	VSS_1	G	Ground	x	
2	N/C		Not used		
3	OUT_1	O	Digital output, open drain	x	
4	TESTANA_2	O	For Test		x
5	MUST1_1	I	For Test		x
6	MUST0_2	I	For Test		x
7	VDD_2	S	Power supply connection		x
8	VDEC_2	S	Regulated Supply		x
9	VSS_2	G	Ground		x
10	OUT_2	O	Digital output, open drain		x
11	N/C		Not used		
12	TESTANA_1	O	For Test	x	
13	MUST1_1	I	For Test	x	
14	MUST0_1	I	For Test	x	
15	VDD_1	S	Power supply connection	x	
16	VDEC_1	S	Regulated Supply	x	

5. Absolute Maximum Ratings

Parameter	Value
Supply Voltage, Vdd	18 V
Reverse Voltage Protection	- 10 V
Reverse Output Current	400 µA
Operating Ambient Temperature Range, T_A	-40°C .. 125 °C
Storage Temperature Range, T_S	-50°C .. 125 °C
Storage time	10 years
Processability Time - Note 1)	2 years

Note: 1) Time counted from package date code during which the correct process ability is guaranteed.

Exceeding the absolute maximum ratings may cause permanent damage. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

6. MLX90292 Electrical Specifications

DC Operating Parameters at Vdd = + 6V and for T_A = – 40°C… + 125°C (unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply Voltage						
Operating Supply Voltage	Vdd		4.6		8.7	V
Regulated Supply Voltage	Vdec	Note 1)	3.0		3.6	V
Por Level	POR	Refer to Vdig	2.5		3.3	V
Por Level Hysteresis	PORHY		0.1			
Supply Current normal operation (PAS4 & PWM)						
Nominal, Idd_{low}	Idd_{low}		13		19	mA
Iddhigh1	Idd_{high1}	high level with 200Ω between OUT and Vdd.	43 43		90 64	mA mA
Supply Current optional operation (PSI5-A)						
Nominal, Idd_{low}	Idd_{low}		-		19	mA
Delta_I	Delta_Idd	high level with 920Ω between OUT and Vdd	22		30	mA
Startup Level (related to external Vdd, Pin1)						
Startup level	SU_{high}			4.4	4.6	V
Startup Hysteresis	SU_{hys}	Note 2)	0.5		1.0	V
Startup Time						
Startup Time	$t_{startup}$	Note 3)			15	ms
Switch point for Extra Internal current for PAS4 (related to external Vdd)						
Switch point	SP		6			V
Switch point Hysteresis	SPhys		0.3		1	V
Programming Entry level						
Programming Supply Voltage	Vddprog	Start of programming	9.5			V
Programming Supply Voltage Hysteresis	Vddproghys			0.3		V

Notes: 1) Supply for IC, external connection to capacitor only
2) The Hysteresis voltage is specified as measured in test mode; in application the value is approximately reduced by the Idd_{high1} multiplied by the line resistance.
3) Time elapsed between Startup and First Data package sending

7. MLX90292 Pin Specifications

DC Operating Parameters at Vdd = +6V and for T_A = – 40°C… + 125°C (unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Digital Outputs Open Drain (Pull-up Resistor needed)						
Compliance current	Icompl	Driver ON, V_{OUT}= +6V		55		mA
Compliance Voltage	Vcompl1	Driver OFF, Max allowed voltage on OUT = 14V			13	V
Saturation Voltage	Vsat	Driver ON Iout= 50mA		0.2	0.8	V
Leakage Current	Ileak	Driver OFF – Vout = Vpullup = 8V		1	100	µA

8. Timing Specification PAS4 / PSI5-A

DC Operating Parameters at Vdd = +6V and for T_A = – 40°C… + 125°C (unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Clock deviation	CLK_{dev}		-5		5	%
Fall/Rise Time Current Slope	$T_{fall-rise}$	Strongly depends on external components, 20%..80% (of < Idd)	100	200	300	ns
Mark/Space Ratio	Ratio	$(T_{fall,80} – T_{rise,20}) / T_{BIT}$ $(T_{fall,20} – T_{rise,80}) / T_{BIT}$	47	50	53	%
Normal operation						
Frame update rate	Framerate		1.9	2	2.1	kHz
Signal latency	Sig_{lat}	Note 1)	342	380	418	µs
Transmission Speed	TR_{speed}		238	250	262	kbit / s
Bit Time	T_{BIT}	Note 4)	3.8	4	4.2	µs
Half Bit Time	T_{Bhalf}	Note 4)	1.9	2	2.1	µs
Frame Gap Time	T_{FGAP}	T_{GAP} >T_{BIT} Note 2)	4.2	8		µs
Package Gap Time	T_{PGAP}	Note 2)	254	268	282	µs
Optional operation						
Frame update rate	Framerate		0.95	1	1.05	kHz
Signal latency	Sig_{lat}	Note 1)	796	884	972	µs
Transmission Speed	TR_{speed}		119	125	131	kbit / s
Bit Time	T_{BIT}	Note 4)	7.6	8	8.4	µs
Half Bit Time	T_{Bhalf}	Note 4)	3.8	4	4.2	µs
Frame Gap Time	T_{FGAP}	T_{GAP} >T_{BIT} Note 3)	8.4	16		µs
Package Gap Time	T_{PGAP}	Note 3)	508	536	564	µs

Note:

1) Signal latency is defined as the time between the second half of the sampling integration time interval of the Hall plate voltage and the transmission of the last bit of the data package
2) See Figure 2.
3) See Figure 3.
4) See Figure 4.

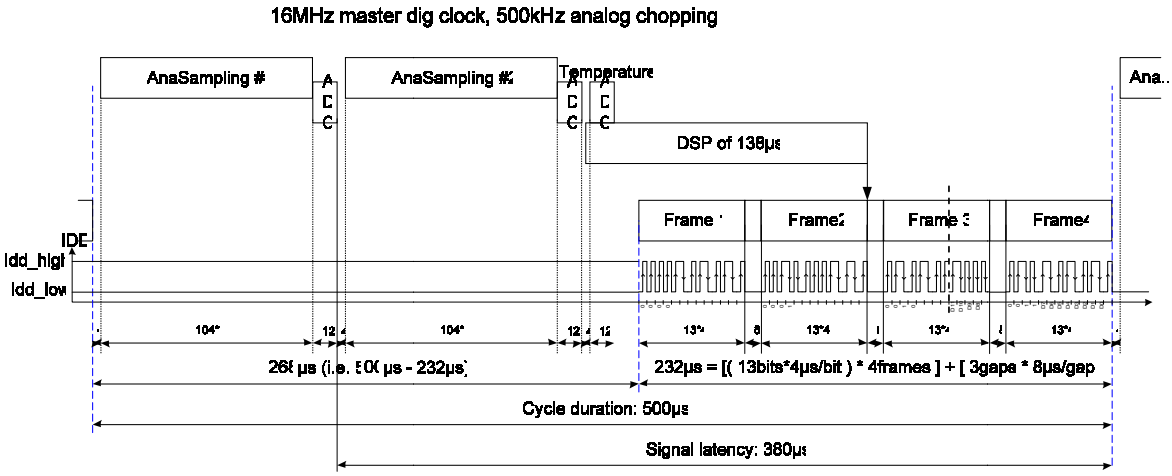


Figure 2: Signal timing (frame), PAS4/PSI5-A normal operation

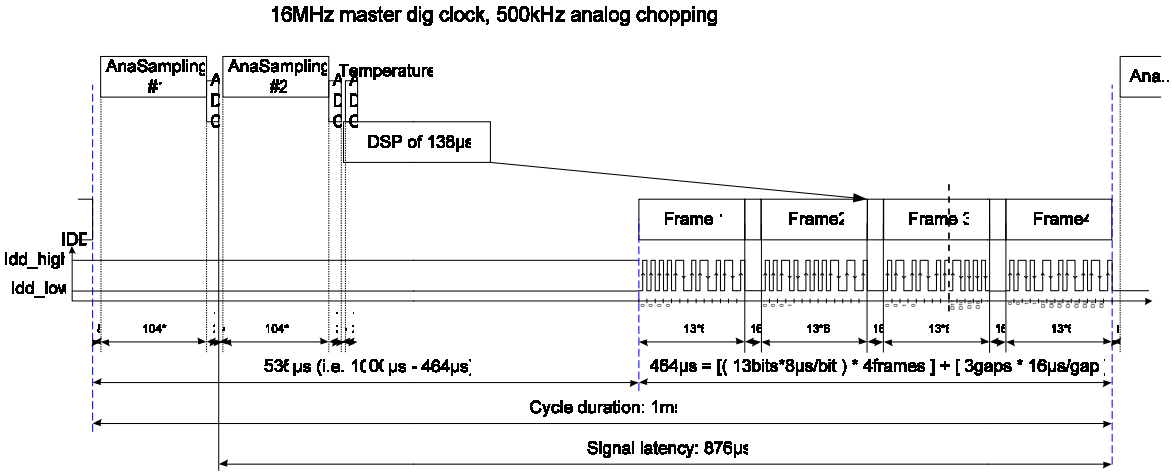


Figure 3: Signal timing (frame), PAS4/PSI5-A optional operation.

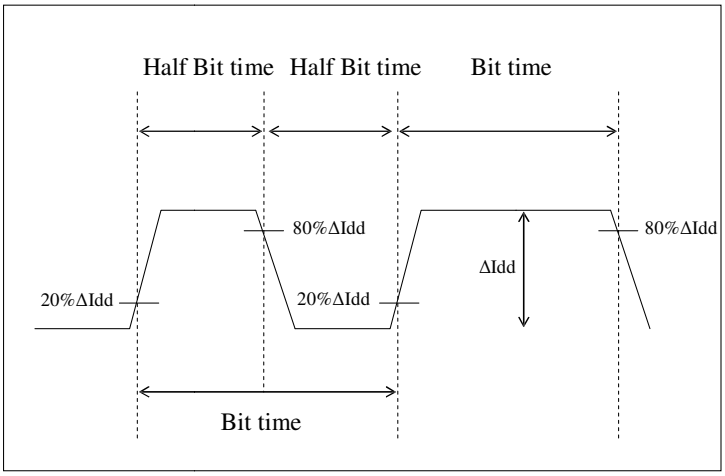


Figure 4: Bit Time definitions.

9. Timing Specification PWM

DC Operating Parameters at Vdd = + 6V and for T_A = – 40°C… + 125°C (unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Fall/Rise Time Current Slope	$T_{fall-rise}$	Strongly depends on external components, 20%..80% (of < Is)	100		300	ns
Normal PWM operation						
PWM frequency	PWM_Freq	with EE_PWM_Freq = 0 or 7	1.8	2	2.2	kHz
		with EE_PWM_Freq = 1	0.9	1	1.1	kHz
		with EE_PWM_Freq = 2	450	500	550	Hz
		with EE_PWM_Freq = 3	360	400	440	Hz
		with EE_PWM_Freq = 4	225	250	275	Hz
		with EE_PWM_Freq = 5	180	200	220	Hz
		with EE_PWM_Freq = 6	112	125	138	Hz
Signal Latency (note 1)	Sig_{lat}	with EE_PWM_Freq = 0 or 7	792	880	968	µs
		with EE_PWM_Freq = 1	1.692	1.88	2.068	ms
		with EE_PWM_Freq = 2	3.492	3.88	4.268	ms
		with EE_PWM_Freq = 3	4.392	4.88	5.368	ms
		with EE_PWM_Freq = 4	7.092	7.88	8.668	ms
		with EE_PWM_Freq = 5	8.892	9.88	10.87	ms
		with EE_PWM_Freq = 6	14.29	15.88	17.47	ms
PWM upper diagnostic Range	Diag_High			98		%
PWM lower diagnostic Rangel	Diag_Low			2		%
PWM signal operating Range	Sig_Range	Note 2)	3		97	%
PWM Resolution	PWM_Res			12		Bits

Note: 1) Signal latency is defined as the time between the second half of the sampling integration time interval of the Hall plate voltage of cycle N and the end of the next PWM cycle N+1.
2) Represents the value of the Duty Cycle

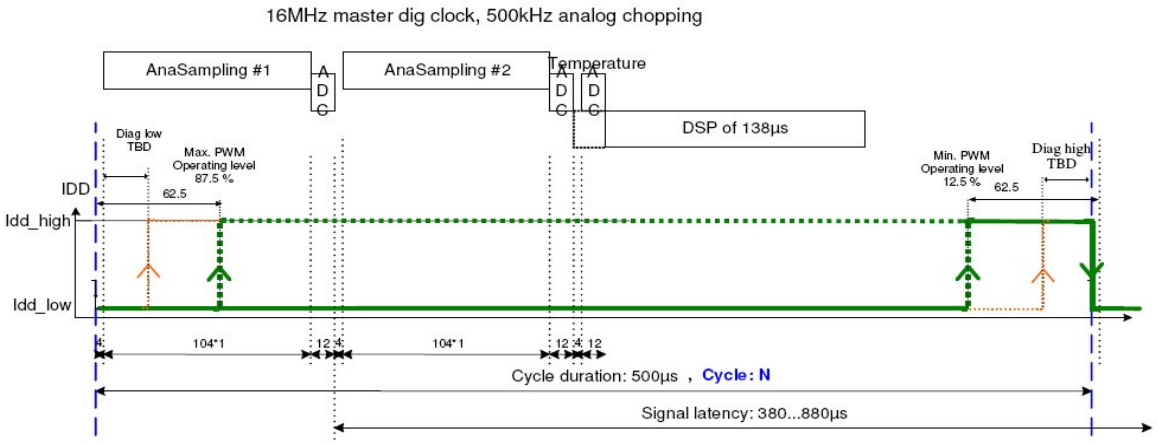


Figure 5: Signal timing (frame), PWM operation

10. Sensor Specifications

DC Operating Parameters at Vdd = + 6V and for T_A = – 40°C… + 125°C (unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Magnetic Sensor						
Linearity error	LinG	Note 1)		0.2		%
Effective number of bits	$Bits_{eff.}$	No Filter active	9.4	10		bits
Offset Drift	B_{drift}	Note 1)			37	LSB_{12}
Gain Drift	G_{drift}	Note 1)	-2		2	%
Gain Aging	G_{aging}		-0.5		0.5	%
Sensitivity range	F_{range}	Field Range	+/- 30		+/- 170	mT
Thermometer						
Temperature Range	T_{range}		-50		155	°C
Temperature accuracy	T_{acc1}		-10	0	+10	°C
Temperature resolution	$T_{resolution}$	8 bits		0.8		°C

Note:

1) The linearity error is the signal deviation (full scale) to the regression line
2) The offset error is the signal deviation (Full scale) at zero field.
3) The Gain drift is the deviation from the Gain nominal value (0h; 25°C).

11. Description of the MLX90292 functions/blocks

11.1. Filtering

The MLX90292 has a build in filter which takes care of the suppression of the signal noise. For the reason of trade-off between signal dynamics the filtering is programmable. A FIR filtering will be used for this, which enables several cut-of frequencies and signal latencies.

11.2. Self Test

The MLX90292 has some build in self-test features, which check the RAM, ROM, EEPROM for its correct storage function. The MLX90292 has also a watch-dog. The ROM and EEPROM are checked during operation, this is a background process. The duration of one check is 100ms.

11.3. POR

The POR is needed for the reset of the analog part and digital part of the MLX90292.The POR is supplied by the internally regulated supply Vdec. There is no built-in delay on the POR circuitry (such as debouncing), so the POR is designed to put the IC in reset whenever the regulated supply falls below a specified threshold.

11.4. Charter of Functional Status

Range	Voltage (V)	Current	Functional status
Reverse Voltage	0 … -10	Below 400 µA normal IC	C
Idle	0 … 2,7	<IddLow max	C
POR Transition	2,7 … 4,8	<IddHigh max	C A
Normal	4,8 … 8.9	<IddHigh max	A
Over Voltage Transition	8.9 … 9.5	Mixture from Idd low and Idd high.	A C
Safety in overvoltage range	> 9.5	Programming Idd modulation	C

12. EEPROM

12.1. Table of content

MELEXIS PARAMETERS		
Parameter	Number of Bits	Description
MLXLOCK	8	Melexis EEPROM area lock byte
DISEECRC	8	Disable the EEPROM CRC check
MLXCALIBMODE	8	Calibration mode selection
MLXCONFIG	8	Configuration settings for the digital
THERMOOFFS25	15	Temperature sensor offset trimming
THERMOSLOPEHOT	16	Temperature sensor thermal drift at hot trimming
THERMOSLOPECOLD	16	Temperature sensor thermal drift at cold trimming
MLXOK	1	Calibration successful flag
OSCTRIM	5	Oscillator frequency trimming
EXTRAIDDLOW	2	Idd_low trimming for PAS4 mode
ANASAMPLES	2	Analog sampling time trimming
ANADURATION	2	Analog integration duration trimming
EXTRAIDDHIGHPSI	3	Idd_high trimming in PSI5 mode for low Vdd
ITRIM	4	ASIC current reference trimming
IPLATE	4	Hall plate temperature independent biasing current
TRIMCTAT	5	Temperature dependent current source trimming
EXTRAIDDHIGHPAS	3	Idd_high trimming in PAS4 mode for low Vdd
TC1ST	7	Hall plate current biasing trimming
PLATEPOL	1	Polarity of the Hall plate biasing
TC2ND	5	Hall plate current biasing trimming
MLXOFFSET	16	Temperature independent offset correction factor
OFFSLOPEHOT	16	Thermal offset drift compensation at hot
OFFSLOPECOLD	16	Thermal offset drift compensation at cold
SENSSLOPEHOT	16	Thermal sensitivity drift compensation at hot
SENSSLOPECOLD	16	Thermal sensitivity drift compensation at cold
MLXID0	16	Melexis identification number
MLXID1	16	Melexis identification number
MLXID2	16	Melexis identification number

CUSTOMER PARAMETERS		
Parameter	Number of Bits	Description
PCUSTID0	16	Primary customer identification number
PCUSTID1	16	Primary customer identification number
PCUSTID2	16	Primary customer identification number
PCUSTLOCK	8	Primary customer EEPROM area lock byte
DIEID	1	Indication of die in the dual-die package
PWMPOL	1	PWM polarity bit

OPM	3	Operation mode determining output protocol
PCOK	1	Calibration successful flag
FILTER	4	FIR filter selection
PWMFREQ	3	PWM frequency
THERMOOFFSETCORR	8	Temperature sensor offset correction
THERMOHOTCORR	16	Temperature sensor drift at hot correction
THERMOCOLDCORR	16	Temperature sensor drift at cold correction
MANUFCOUNTVALUE	8	Number of manufacturing data packages at startup
TA	15	Temperature pivot point between TC1hot and cold
TCSENSHOT	16	Thermal sensitivity drift compensation for T>TA
TCSENSCOLD	16	Thermal sensitivity drift compensation for T<TA
TCOFFSET	16	Temperature drift compensation of the offset
PCUSTPARAM0	16	Free parameter

END CUSTOMER PARAMETERS		
Parameter	**Number of Bits**	**Description**
ECUSTLOCK	8	End customer EEPROM area lock
ECOK	1	Calibration successful flag
S3	1	PAS4/PSI5 data package information bit
ROUGHGAIN	3	Analog gain
DIAGSIDE	2	Defines the diagnostics' duty cycles in PWM mode
ECUSTOFFSET	16	Offset correction factor
XA	14	Sensitivity S-curve pivot point
TOOBENABLE	2	Defines if temperature out of bounds detection is enabled in PWM mode
SLOPE1	16	Sensitivity in the range [-XA .. XA]
SLOPE2	16	Sensitivity outside the range [-XA .. XA]
SLOPE3	16	Sensitivity for B < -XA only in PWM mode
CLAMPLOW	16	Low clamping value (only useful in PWM mode)
CLAMPHIGH	16	High clamping value (only useful in PWM mode)
TOOBLOW	8	Low temperature threshold for PWM diagnostics
TOOBHIGH	8	High temperature threshold for PWM diagnostics
ECUSTPARAM0	16	Free parameter
ECUSTPARAM1	16	Free parameter
ECUSTPARAM2	16	Free parameter
ECUSTPARAM3	16	Free parameter
ECUSTPARAM4	16	Free parameter
ECUSTPARAM5	16	Free parameter
ECUSTPARAM6	16	Free parameter
ECUSTPARAM7	16	Free parameter
ECUSTID0	16	Free parameter
ECUSTID1	16	Free parameter
ECUSTID2	16	Free parameter
CRC	16	EEPROM Cyclic Redundancy Check

12.2. EEPROM Lock-mechanism

In order to support longer supply chains due to sequential assembly, the EEPROM space has been divided in 3 areas. There is 1 byte for each of the 3 EEPROM areas in the EEPROM to control area locking:

- The Melexis part: MLXLOCK
- The Primary Customer part: PCUSTLOCK
- The End Customer part: ECUSTLOCK

In case these lock bytes are 00h, the customer further down the supply chain can still modify the EEPROM area of its supplier. In case the locks are written, the customer will only have access to his part of the EEPROM. It is possible to only lock a part of the EEPROM by writing a non-zero value in the lock byte. By writing 06h in EEPROM, the first 6 addresses of that EEPROM area are write-protected, but the other addresses remain accessible.

Some unlock keys are available when using the programming equipment to overrule these EEPROM lock bytes.

13. Interfaces

The MLX90292 supports multiple output protocols. At one side of the spectrum there are the PAS4 and PSI5-A digital protocols, which mainly differ from one and other through the value of the resistive pull-up resistor on the open-drain output. This difference has an impact on the specifications of both protocols when it comes to defining the range of the low and high currents:

- PAS4 specifies a separate range for both the Idd_low and Idd_high
- PSI5-A specifies a range on the difference between Idd_low and Idd_high, i.e. on Idd_delta

The other type of communication protocol is PWM. Here as well, a 2-wire variant exists which requires pull-up resistors in the range of the PAS4/PSI5-A protocols in order to accommodate a good noise margin between both levels? Then there is also the conventional 3-wire PWM protocol that supports the typical higher impedant pull-up values such as 4K7 ohms and 10K ohms. The demodulation at receiver side is then no longer current based, but becomes voltage based. The user can select the desired communication protocol via EEPROM, through the parameter OPM.

13.1. PAS4 / PSI5-A Interface

The interface PAS4 / PSI5-A is a unidirectional asynchronous digital current (two-wire) interface. It is used for point-to-point connections in automotive environments. Timing and repetition rate of the data transmission are controlled by the device. The user can program both 1kHz and 2kHz data rate. Data transmission from the device to the ECU is done by current modulation on the power supply lines. When no data package is sent, i.e. the interface is in idle mode, the interface shall draw no current additional to the supply current (Idd_low) in order to prevent unnecessary heating of the device.

13.1.1. Protocol: Manchester Code

Data transmission is done in Manchester code. This ensures that in the middle of each bit an edge is present, allowing the receiver ECU to synchronize easily on the transmissions of the Hall IC.

Transmission is also quite insensitive to tolerances of the oscillator frequency. A logic "1" is represented with a falling Idd edge in the middle of the bit. A logic "0" is represented with a rising Idd edge in the middle of the bit. See also Figure 6

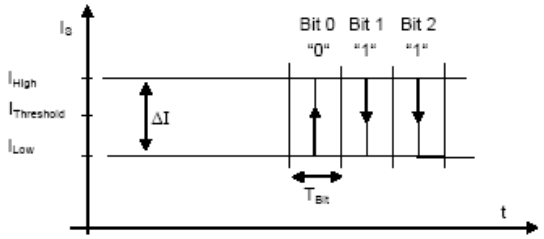


Figure 6: Manchester code

One frame consists of 13 bits. All frames start with two bits logic"=0". The two following bits identify the frame number inside one data package. There are 4 frames per package, and the datarate is specified as packages per unit of time. At the end of every frame a parity bit is generated. Odd/even parity is used depending on the type of package (measurement data or manufacturing data), so the receiver has the ability to detect 1 error per frame. The encoder generates the appropriate timing for the messages to be sent and controls the communication interface accordingly. For an example see also Figure 7. For a gap time between two frames see chapter 8.

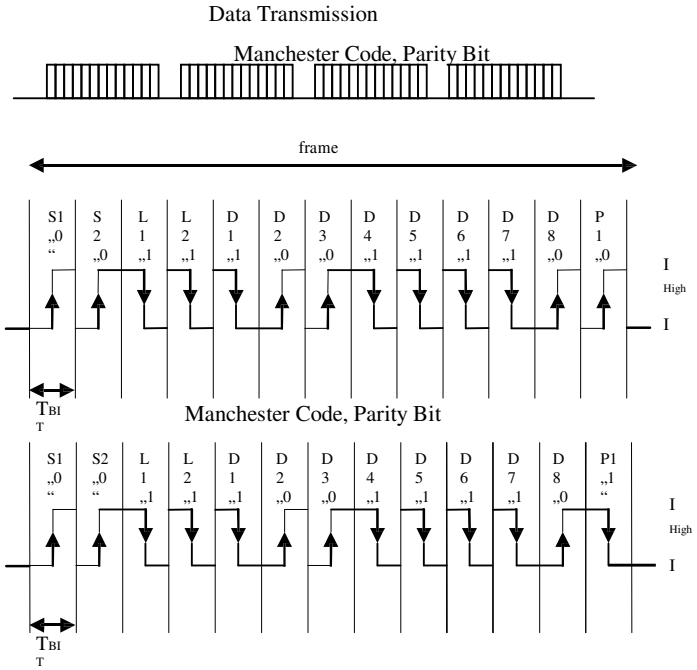


Figure 7: Example data frames

13.1.2. Data Packages

Two types of data packages exist:

- Manufacturing data package
- Measurement data package

13.1.2.1. Manufacturing Data Package

The manufacturing package contains the values of the EEPROM registers. The values are transmitted in byte data format. The initial manufacturing package contains two bytes, the following packages contain three bytes of EEPROM data. A manufacturing data package consists of 4 frames each having a label for identification. An odd parity bit is used for detection of transmission errors. The initial manufacturing package includes the error and status information in the second frame. The following packages only have an OK information bit followed by the package counter and three bytes containing the EEPROM information. With the counter a failure of the package transmission order can be detected. With the help of the counter the data can be allocated to the EEPROM registers. The package counter starts with the first package, giving the receiver the possibility to detect if a certain package was lost, and thus the ability to reconstruct a proper EEPROM table. The MANUF_COUNT_VALUE parameter in EEPROM defines the number of data packages that will be transmitted at startup. Startup in this case is defined as coming out of reset, i.e. out of POR. In case the supply was below the startup voltage, but still above the POR threshold, and goes back to the normal operating range, the measurement data packages will be resumed without sending manufacturing data packages first.

Initial Manufacturing Data Package													
	St2	St1	W2	W1	D7	D6	D5	D4	D3	D2	D1	D0	P0
1	0	0	1	1	0	1	OK	C4	C3	C2	C1	C0	o
2	0	0	1	0	ID	X2	X1	X0	S3	S2	S1	S0	o
3	0	0	0	1	0	0	0	0	0	0	0	0	o
4	0	0	0	0	N7	N6	N5	N4	N3	N2	N1	N0	o
	12	11	10	9	8	7	6	5	4	3	2	1	0

Package 2 … n-1													
	St2	St1	W2	W1	D7	D6	D5	D4	D3	D2	D1	D0	P0
1	0	0	1	1	0	1	OK	C4	C3	C2	C1	C0	o
2	0	0	1	0	D_{205B} MSB	D_{205B}	D_{205B}	D_{205B}	D_{205B}	D_{205B}	D_{205B}	D_{205B} LSB	o
3	0	0	0	1	D_{205A} MSB	D_{205A}	D_{205A}	D_{205A}	D_{205A}	D_{205A}	D_{205A}	D_{205A} LSB	o
4	0	0	0	0	D_{2059} MSB	D_{2059}	D_{2059}	D_{2059}	D_{2059}	D_{2059}	D_{2059}	D_{2059} LSB	o
	12	11	10	9	8	7	6	5	4	3	2	1	0

Last Manufacturing Data Package													
	St2	St1	W2	W1	D7	D6	D5	D4	D3	D2	D1	D0	P0
1	0	0	1	1	0	1	OK	C4	C3	C2	C1	C0	o
2	0	0	1	0	CRC MSB	CRC	CRC	CRC	CRC	CRC	CRC	CRC	o
3	0	0	0	1	CRC	CRC	CRC	CRC	CRC	CRC	CRC	CRC LSB	o
4	0	0	0	0	0	0	0	0	0	0	0	0	o
	12	11	10	9	8	7	6	5	4	3	2	1	0

St2,St1 = Two consecutive start bits, always zero

W = Label for frame identification

frame 1: Label = <1 1>
frame 2: Label = <1 0>
frame 3: Label = <0 1>
frame 4: Label = <0 0>

N = Number of sent packages – 2 (initial and last packages are always sent)

OK = OR-ing of the error bits except for the ADC over-/underflows
So the OK bit can become 0 if one of the following errors occurs:

- RAM check fail: the RAM march failed or the RAM vs EEPROM check failed (if enabled)
- ROM CRC fail
- EEPROM CRC fail
- WD acknowledge error

C = 5-bit package counter for package identification

Package 1: package counter = <00000>
Package 2 package counter = <00001>
….
Package 32 package counter = <11111>

P = Odd parity over frame bits 1 … 12 (= all other bits, including start bits)

ID = Identification of the die position within the dual-die package

ID = 0: then IC is mounted closest to pin #1
ID = 1: then IC is mounted farthest from pin #1

X = Error detection

X2	X1	X0	Error interpretation
0	0	0	No error detected
0	0	1	ADC Overflow
0	1	0	ADC Underflow
0	1	1	PAS4 / PSI5 not ready
1	0	0	RAM check
1	0	1	Watchdog acknowledge (Software-watchdog)
1	1	0	CRC Fail ROM
1	1	1	CRC Fail EEPROM

Error detection reporting specification

Phase	Integrity Test	Description	Action on Fail
StartUp cycle	RAM Test	Write a fix Data pattern in the RAM and read back for consistency check	Reporting Error Only
	EEPROM CRC	Calculate the EEPROM CRC and compare with the stored CRC	Reporting Error Only
	RAMCMP	Compare the RAM calibration Data with the EEPROM calibration Data	Reporting Error Only
Background	ROM CRC	Calculate the ROM CRC and compare with the stored CRC	Reporting Error Only
	RAMCMP	Compare the RAM calibration Data with the EEPROM calibration Data	Reporting Error Only
	EEPROM CRC	Calculate the EEPROM CRC and compare with the stored CRC	Reporting Error Only

Note 1: The RAM MARCH test error will be reported/flagged in the first frame only; then cleared and never reported/flagged again since the test is never run again (unless a POR occurs).

The ROM CRC, RAMCMP and EEPROM CRC errors will be reported/flagged once after their detection, then once any time they are re-detected.

ALL errors are ONLY reported, i.e. no other actions are taken (Like resets, etc...)

Note 2: The ROM CRC and EEPROM CRC errors are not necessarily flagged AT EVERY frame, depending on which bits (tests) are set in the MLXCONFIG byte.

CRC = CRC of sent manufacturing data packages (IBM 16 CRC)

S = Status

S3	(ECOK) S2	(PCOK) S1	(MLXOK) S0	Status interpretation
0	0	0	0	No calibration established
0	0	0	1	MLX calibration successful
0	0	1	0	Tbd.
0	0	1	1	PCUST calibration successful
0	1	0	0	Tbd.
0	1	0	1	Tbd.
0	1	1	0	Tbd.
0	1	1	1	ECUST calibration successful
1	0	0	0	Free for end User.
1	0	0	1	Free for end User.
1	0	1	0	Free for end User.
1	0	1	1	Free for end User.
1	1	0	0	Free for end User.
1	1	0	1	Free for end User.
1	1	1	0	Free for end User.
1	1	1	1	Free for end User.

Dxxxx = Data of corresponding EEPROM address.

Example for odd parity:

Frame													
	S2	S1	W2	W1	D7	D6	D5	D4	D3	D2	D1	D0	P0
1	0	0	1	1	0	1	1	0	0	0	1	1	1
2	0	0	1	0	0	1	1	0	0	0	1	1	0
3	0	0	0	1	0	1	1	0	0	0	1	1	0
4	0	0	0	0	0	1	1	0	0	0	1	1	1
	12	11	10	9	8	7	6	5	4	3	2	1	0

13.1.2.2. Measurement Data Package

One data package contains the 12 bit signal of one magnetic flux density measurement and additional status information. A data package is composed of 4 frames each having a label for identification. A parity bit is used for detection of transmission errors. The order of the frame transmission is determined by the label: label <0 0> is sent first, label <0 1> is sent secondly etc …

Frame													
	St2	St1	W2	W1	D7	D6	D5	D4	D3	D2	D1	D0	P0
1	0	0	0	0	0	1	OK	C4	C3	C2	C1	C0	e
2	0	0	0	1	T7	T6	T5	T4	T3	T2	T1	T0	e
3	0	0	1	0	ID	X2	X1	X0	M11	M10	M9	M8	e
4	0	0	1	1	M7	M6	M5	M4	M3	M2	M1	M0	e
	12	11	10	9	8	7	6	5	4	3	2	1	0

S2,S1 = Two consecutive start bits, always zero

W = Label for frame identification

frame 1: Label = <0 0>
frame 2: Label = <0 1>
frame 3: Label = <1 0>
frame 4: Label = <1 1>

OK = OR-ing of the error bits except for the ADC over-/underflows

1 = Sensor OK
0 = Sensor detected Failure

C = 5-bit package counter for package identification

Package 1: package counter = <00000>
Package 2 package counter = <00001>
….
Package 32 package counter = <11111>

T = IC Temperature, internal temperature measurement in UINT8 format (MSB first)
Temperature range = -50°C to +155°C
Temperature resolution = 0,8°C per LSB
Temperature clamping at -50°C and +155 °C

ID = Identification of the die position within the dual-die package
ID = 0: then IC is mounted closest to pin #1
ID = 1: then IC is mounted farthest from pin #1

X = Error detection

X2	X1	X0	Error interpretation
0	0	0	No error detected
0	0	1	ADC Overflow
0	1	0	ADC Underflow
0	1	1	PAS4 / PSI5 not ready
1	0	0	RAM check
1	0	1	Watchdog acknowledge (Software-watchdog)
1	1	0	CRC Fail ROM
1	1	1	CRC Fail EEPROM

M = Magnetic flux density, 12 bit resolution

P = Even parity over frame bits 1 … 12 (= all other bits, including start bits)

Example for even parity:

Frame													
	S2	S1	W2	W1	D7	D6	D5	D4	D3	D2	D1	D0	P0
1	0	0	1	1	0	1	1	0	0	0	1	1	0
2	0	0	1	0	0	1	1	0	0	0	1	1	1
3	0	0	0	1	0	1	1	0	0	0	1	1	1
4	0	0	0	0	0	1	1	0	0	0	1	1	0
	12	11	10	9	8	7	6	5	4	3	2	1	0

13.1.3. Data Ranges

Magnetic flux density: Data range 12bit 2's complement

Decimal value	Hexadecimal
2047	7FFh
1	1h
0	0h
-1	FFFh
-2048	800h

Temperature: Data range 8bit unsigned

Temperature in °C	Decimal value	Hexadecimal
-50	0	00h
0	62	3Eh
25	94	5Eh
155	255	FFh

13.1.4. Continuous Transmission (Normal Operation)

After the reset sequence, the transmission of the EEPROM content will be sent and then the device automatically starts with the continuous operation sequence where the measurement data are sent to the ECU.

Continuous operation can be interrupted at any time by a programming sequence in order to write new parameters into the EEPROM. Note that the new content of the EEPROM is utilized only after a succeeding power-on cycle.

13.1.5. Transmission after Reset (Power-On)

After every reset – conducted through power-on – the device transmits the EEPROM content to the ECU.

13.2. Programming in PWM mode

The full 12-bit digital output span of PAS4/PSI5-A (-2048LSB .. 2047LSB) will be mapped to a PWM duty cycle range of 3% to 97% in software. It is therefore possible to fully program the ASIC while using PAS4/PSI5-A mode, and then change the mode to PWM, knowing the mapping relation between the operating modes. PWM mode thus also has all the slope correction, offset drift compensations and sensitivity drift compensations that also exist in the other modes.

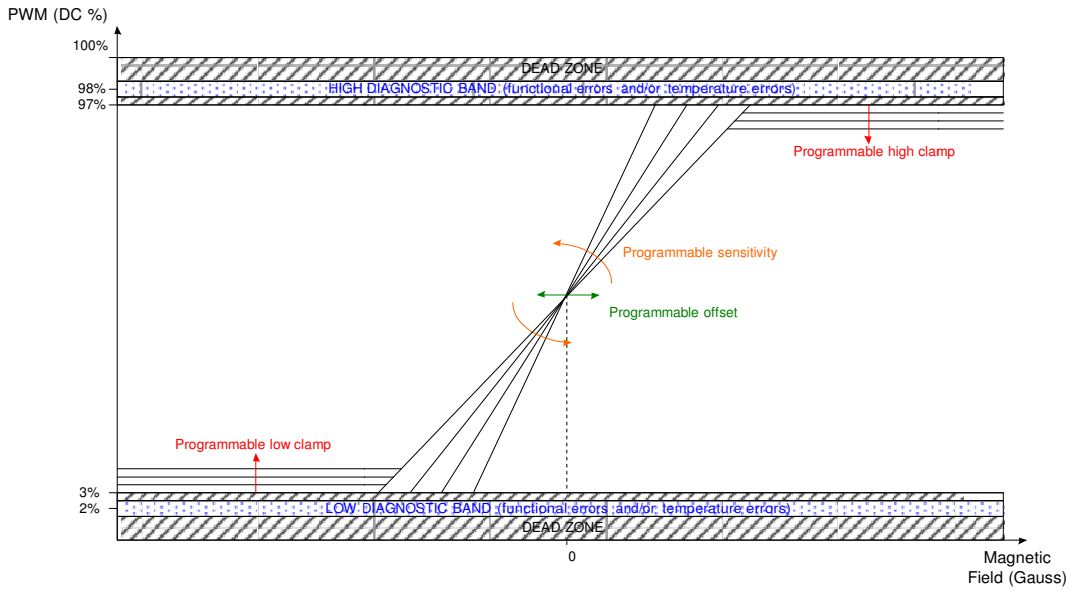


Figure 8: programming in PWM mode

The clamping for PWM differs nothing from the clamping of PAS4/PSI5-A. It takes place on the same digital field data (=PAS4/PSI5-A output data). The clamping settings can be altered in the end customer area of EEPROM. There are 2 parameters available: CLAMP_LOW[15:0] and CLAMP_HIGH[15:0]. The accuracy of the digital field is fixed at 12 bits (-2048 .. 2047), so the clamping can only have the same resolution or less.

Setting your high clamp level at 2000d (=07D0h) will not generate a PWM duty cycle of 50% + (2000/2047)*50% during high clamping. High clamping for those settings will be at 50% + (2000/2047)*47% because the digital field is mapped to a 94% span instead of the full 100%. The same deduction can be made for low clamping. 50% duty cycle always corresponds to digital field 0. The digital field 0 however, can correspond to a certain residual magnetic field depending of the offset value that has been calibrated.

	PWM Duty Cycle (%)	Clamp level (dec)	Internal Value (hex)
Low Clamp Minimum	3	-2048d .. -32768	F800h .. 8000h
Example Low Clamp	10	-1743d	F931h
Example High Clamp	90	1742d	06CEh
High Clamp Maximum	97	2047d .. 32767	07FFh .. 7FFFh

Clamping settings explained

In theory there is no need for clamping, since the digital field is already automatically clamped at 2047 and -2048. For PWM it was made sure that the diagnostic levels were outside this area. However the customer might want to implement a larger dead zone in between the diagnostic levels and the signal span. This can be achieved with the clamping settings, at the price of reduced signal span.

14. Recommended Application Diagrams

14.1. PAS4, PSI5-A and 2-wire PWM

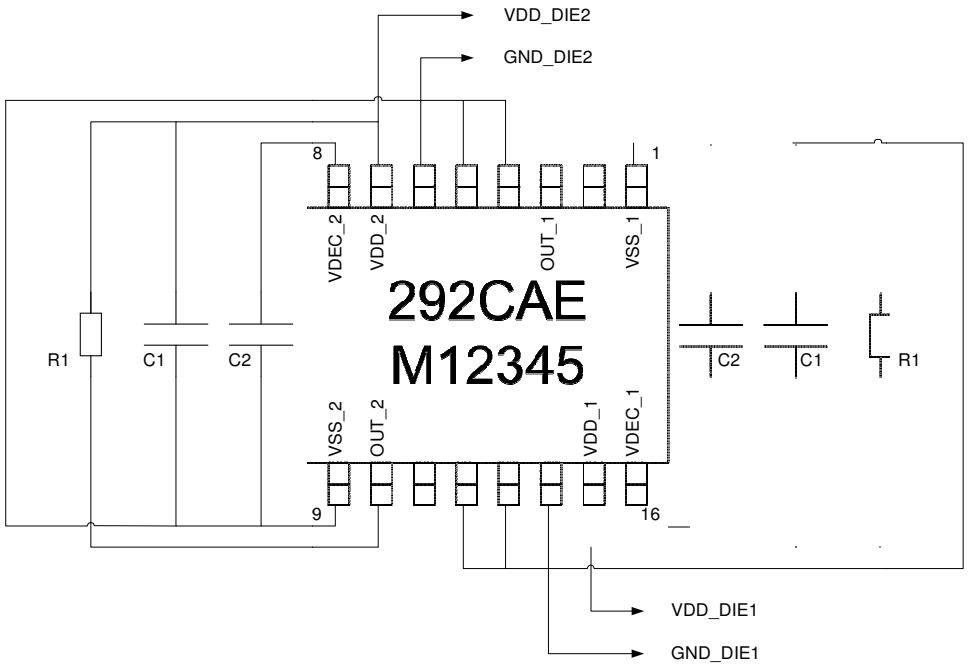


Figure 9: Application diagram PAS4, PSI5-A and 2-wire PWM

Part	Description	Value	Unit
C1	Supply capacitor, EMI, ESD	100	nF
C2	Regulated supply decoupling, EMI, ESD	22	nF
R1	Pull up resistor PAS4	200	Ω
	Pull up resistor PSI5 or 2-wire PWM	920	Ω

14.2. 3-wire PWM

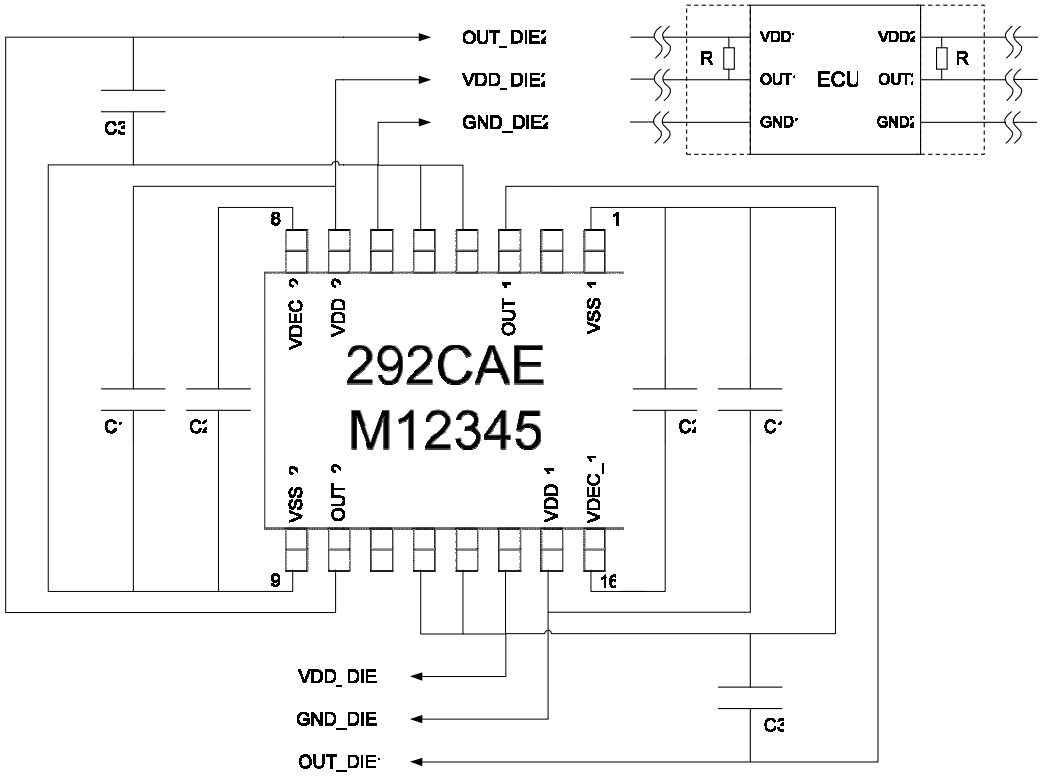


Figure 10: Diagnostic high

Part	Description	Value	Unit
C1	Supply capacitor, EMI, ESD	100	nF
C2	Regulated supply decoupling, EMI, ESD	22	nF
C3	Output capacitor, EMI, ESD	10	nF
R1	Pull up resistor PWM at ECU side	4.7	kΩ

15. Standard information regarding manufacturability of Melexis products with different soldering processes

Our products are classified and qualified regarding soldering technology, solderability and moisture sensitivity level according to following test methods:

Reflow Soldering SMD's (Surface Mount Devices)

- IPC/JEDEC J-STD-020
  Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices
  (classification reflow profiles according to table 5-2)
- EIA/JEDEC JESD22-A113
  Preconditioning of Nonhermetic Surface Mount Devices Prior to Reliability Testing
  (reflow profiles according to table 2)

Wave Soldering SMD's (Surface Mount Devices) and THD's (Through Hole Devices)

- EN60749-20
  Resistance of plastic- encapsulated SMD's to combined effect of moisture and soldering heat
- EIA/JEDEC JESD22-B106 and EN60749-15
  Resistance to soldering temperature for through-hole mounted devices

Iron Soldering THD's (Through Hole Devices)

- EN60749-15
  Resistance to soldering temperature for through-hole mounted devices

Solderability SMD's (Surface Mount Devices) and THD's (Through Hole Devices)

- EIA/JEDEC JESD22-B102 and EN60749-21
  Solderability

For all soldering technologies deviating from above mentioned standard conditions (regarding peak temperature, temperature gradient, temperature profile etc) additional classification and qualification tests have to be agreed upon with Melexis.

The application of Wave Soldering for SMD's is allowed only after consulting Melexis regarding assurance of adhesive strength between device and board.

Melexis is contributing to global environmental conservation by promoting **lead free** solutions. For more information on qualifications of **RoHS** compliant products (RoHS = European directive on the Restriction Of the use of certain Hazardous Substances) please visit the quality page on our website: http://www.melexis.com/quality.aspx

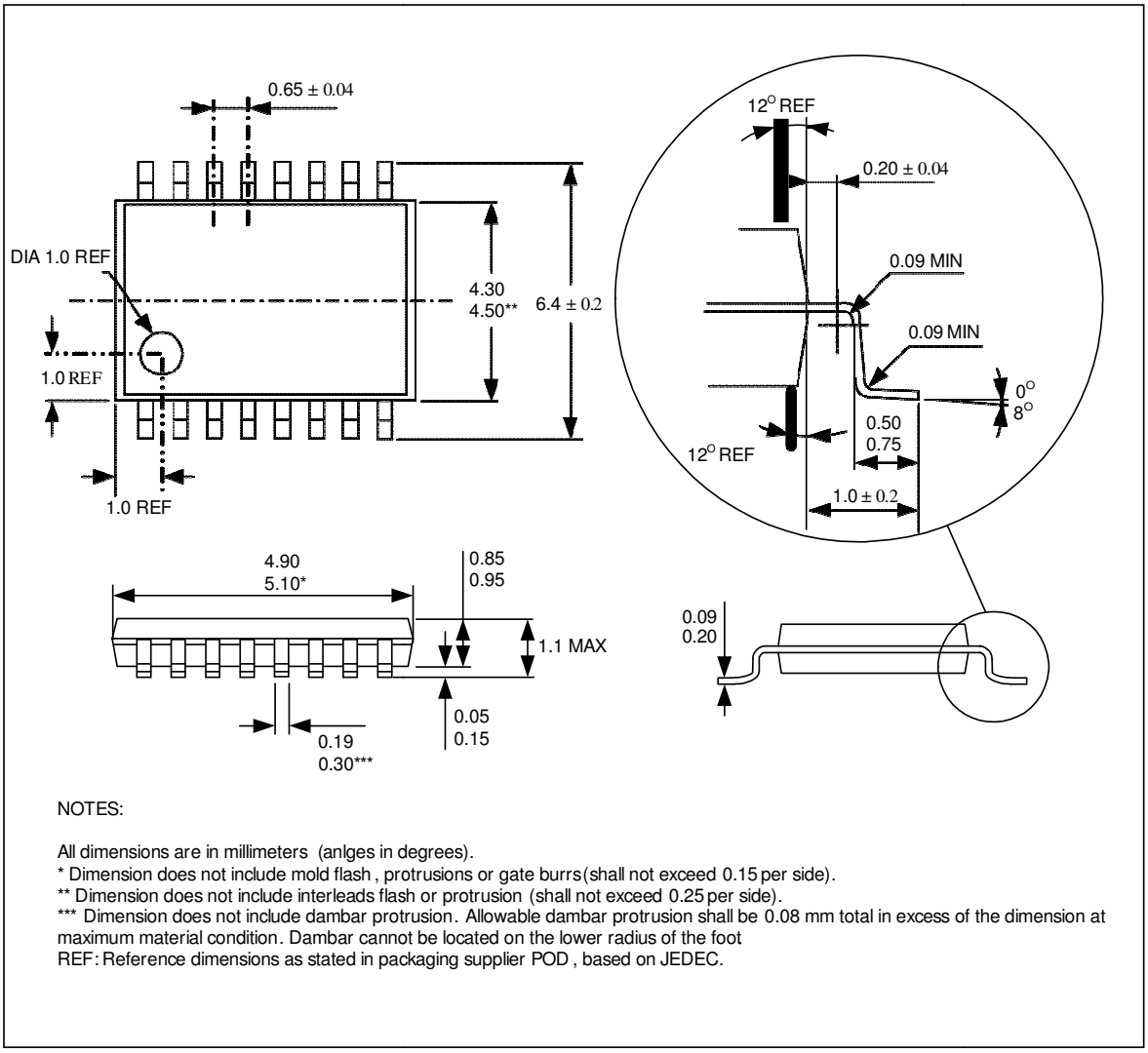
16. ESD Precautions

Electronic semiconductor products are sensitive to Electro Static Discharge (ESD). Always observe Electro Static Discharge control procedures whenever handling semiconductor products.

The target ESD withstand is ± 2 kV for all the combinations specified by AEC-Q100-002 (Human Body Model).

17. Package Information

17.1. TSSOP16 – Package Dimensions



NOTES:

All dimensions are in millimeters (anlges in degrees).
* Dimension does not include mold flash, protrusions or gate burrs (shall not exceed 0.15 per side).
** Dimension does not include interleads flash or protrusion (shall not exceed 0.25 per side).
*** Dimension does not include dambar protrusion. Allowable dambar protrusion shall be 0.08 mm total in excess of the dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot
REF: Reference dimensions as stated in packaging supplier POD, based on JEDEC.

Figure 11: TSSOP16 package dimension

17.2. TSSOP16 – Pinout and Sensitive spot positioning

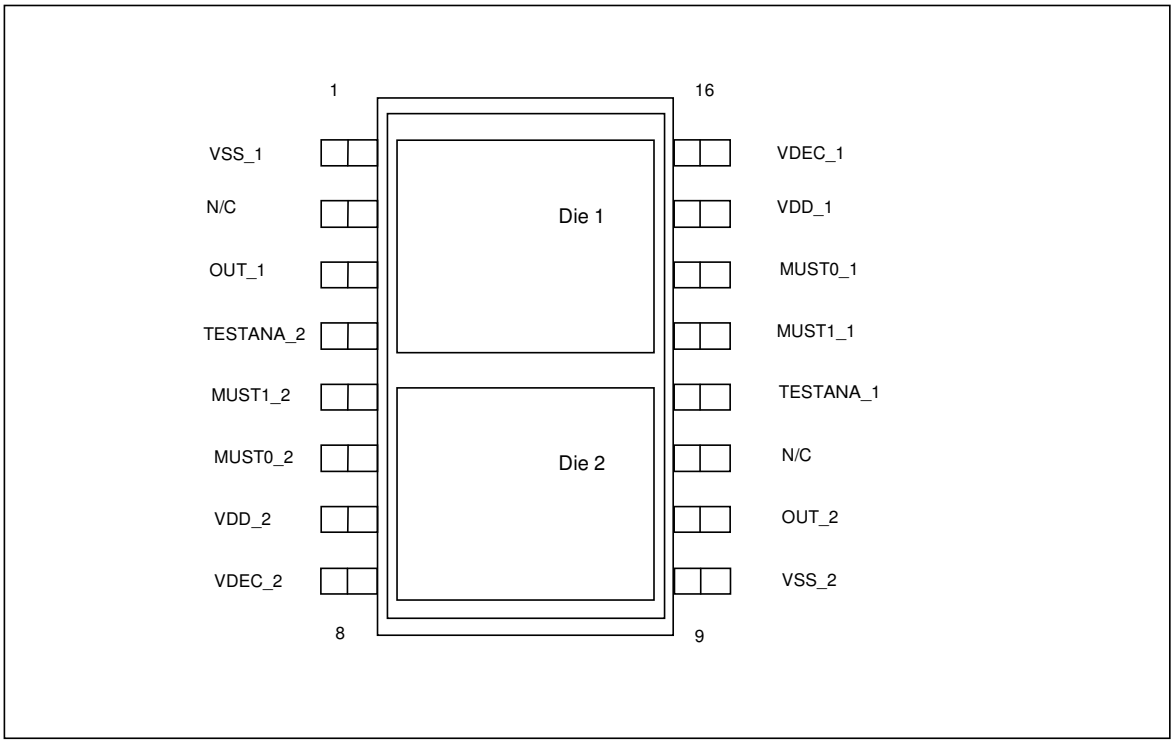


Figure 12: Pinout

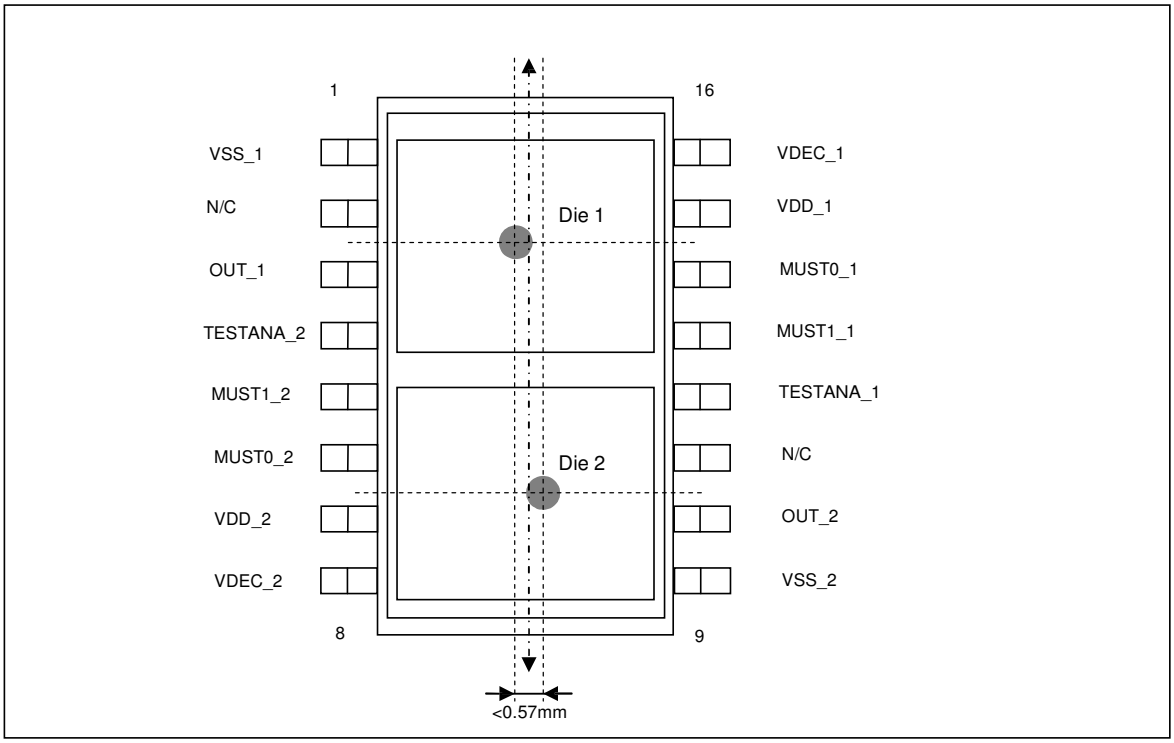


Figure 13: Sensitive spot positioning

18. Disclaimer

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