LH75400/01/10/11
System-on-Chip

DESCRIPTION

The SHARP BlueStreak LH75400/01/10/11 family consists of four low-cost 16/32-bit System-on-Chip (SoC) devices.

- LH75401 — contains the superset of features.
- LH75411 — similar to LH75401, without CAN 2.0B.
- LH75400 — similar to LH75401, but with a Gray-scale LCDC only.
- LH75410 — similar to LH75400, without CAN 2.0B.

COMMON FEATURES

- Highly Integrated System-on-Chip
- ARM7TDMI-S™ Core
- High Performance (84 MHz CPU Speed)
  - Internal PLL Driven or External Clock Driven
  - Crystal Oscillator/Internal PLL Can Operate with Input Frequency Range of 14 MHz to 20 MHz
- 32KB On-chip SRAM
  - 16KB Tightly Coupled Memory (TCM) SRAM
  - 16KB Internal SRAM
- Clock and Power Management
  - Low Power Modes: Standby, Sleep, Stop
- Eight Channel, 10-bit Analog-to-Digital Converter
- Integrated Touch Screen Controller
- Serial interfaces
  - Two 16C550-type UARTs supporting baud rates up to 921,600 baud (requires crystal frequency of 14.756 MHz).
  - One 82510-type UART supporting baud rates up to 3,225,600 baud (requires a system clock of 70 MHz).
- Synchronous Serial Port
  - Motorola SPI™
  - National Semiconductor Microwire™
  - Texas Instruments SSI
- Real-Time Clock (RTC)
- Three Counter/Timers
  - Capture/Compare/PWM Compatibility
  - Watchdog Timer (WDT)
- Low-Voltage Detector
- JTAG Debug Interface and Boundary Scan
- Single 3.3 V Supply
- 5 V Tolerant Digital I/O
  - XTALIN and XTAL32IN inputs are 1.8 V ± 10%
- 144-pin LQFP Package
- -40° C to +85° C Operating Temperature

Unique Features of the LH75401

- Color and Grayscale Liquid Crystal Display (LCD) Controller
  - 12-bit (4,096) Direct Mode Color, up to VGA
  - 8-bit (256) Direct or Palletized Color, up to SVGA
  - 4-bit (16) Direct Mode Color/Grayscale, up to XGA
  - 12-bit Video Bus
  - Supports STN, TFT, HR-TFT, and AD-TFT Displays.
- CAN Controller that supports CAN version 2.0B.

Unique Features of the LH75411

- Color and Grayscale LCD Controller (LCDC)
  - 12-bit (4,096) Direct Mode Color, up to VGA
  - 8-bit (256) Direct or Palletized Color, up to SVGA
  - 4-bit (16) Direct Mode Color/Grayscale, up to XGA
  - 12-bit Video Bus
  - Supports STN, TFT, HR-TFT, and AD-TFT Displays.

Unique Features of the LH75400

- Grayscale LCDC
  - 4-bit (16 Level) Grayscale, up to XGA
  - 8-bit Video Bus
  - Supports STN Displays.
- Controller Area Network (CAN) Controller that supports CAN version 2.0B.

Unique Features of the LH75410

- Grayscale LCDC
  - 4-bit (16 Level) Grayscale, up to XGA
  - 8-bit Video Bus
  - Supports STN Displays.

NOTES:
1. ARM7 Thumb, and ARM7TDMI-S are trademarks of ARM LTD.
2. Motorola SPI is a trademark of Motorola, Inc.
3. Microwire is a trademark of National Semiconductor Corporation.
4. VGA and XGA modes require 66 MHz CPU speed.
5. XTAL inputs are not 5 V tolerant.
6. CPU performance at 1.8 V at 50°C, VDDC supplied externally.

LH75401 BLOCK DIAGRAM

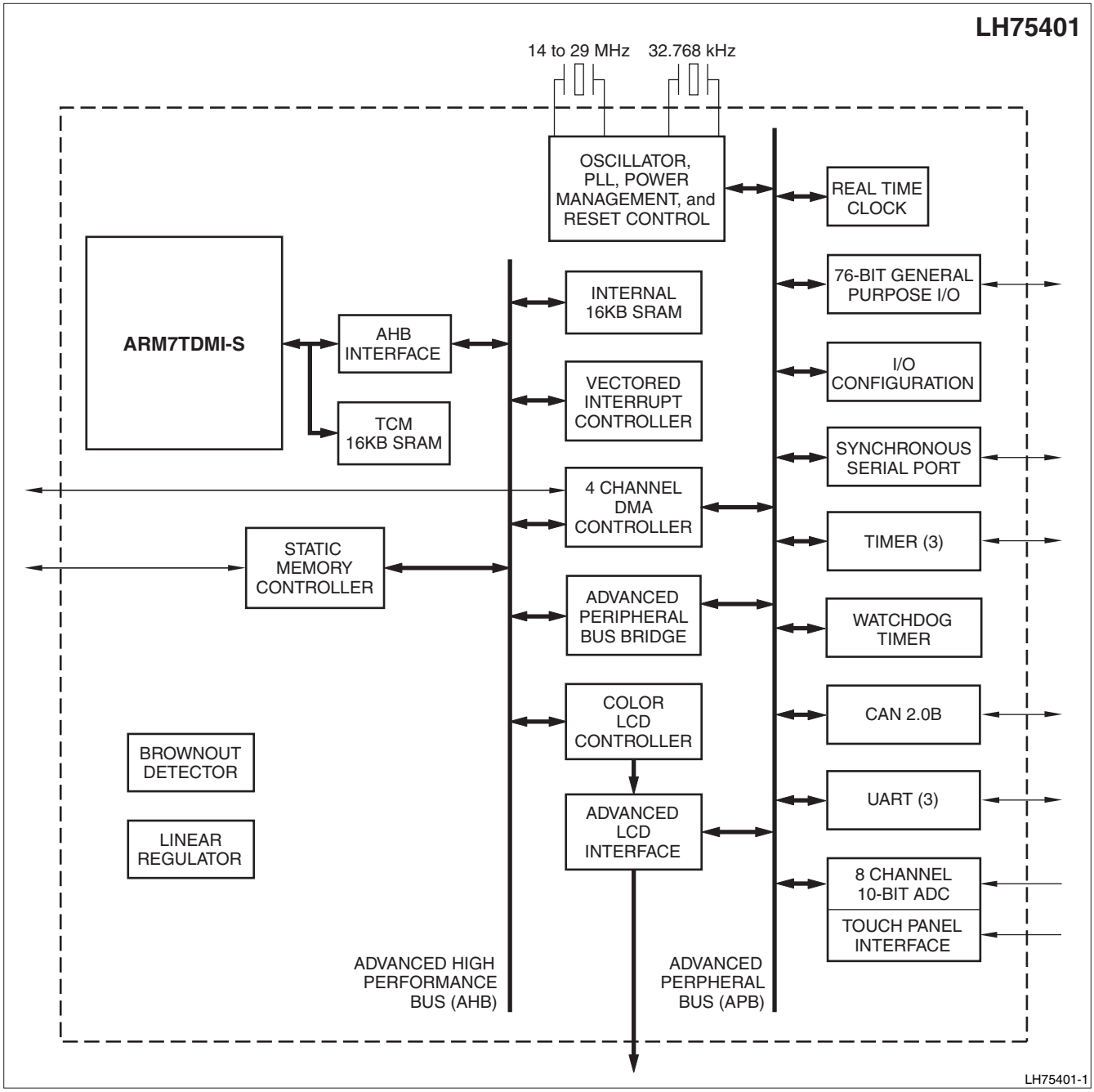


Figure 1. LH75401 Block Diagram

LH75411 BLOCK DIAGRAM

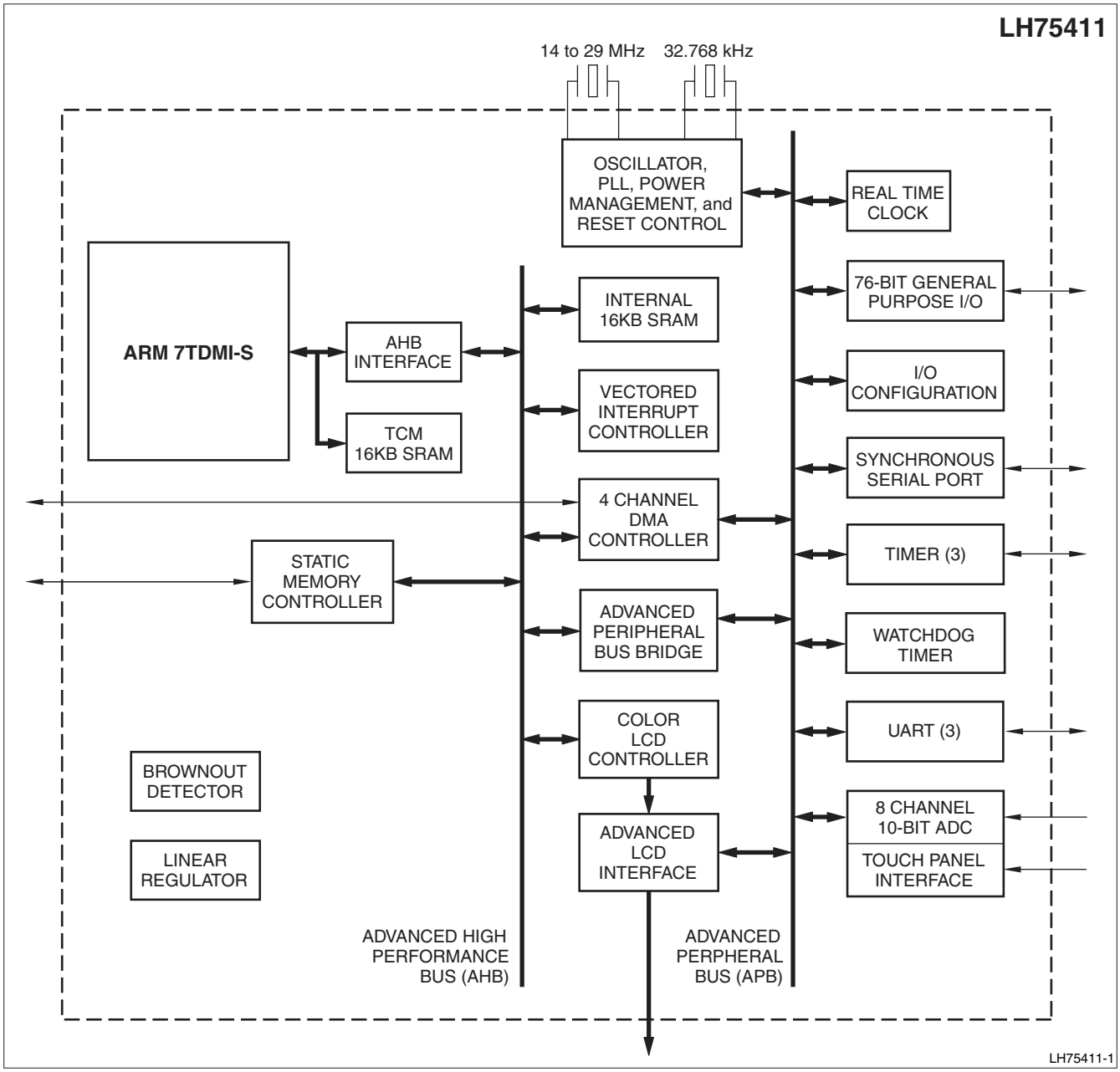


Figure 2. LH75411 Block Diagram

LH75400 BLOCK DIAGRAM

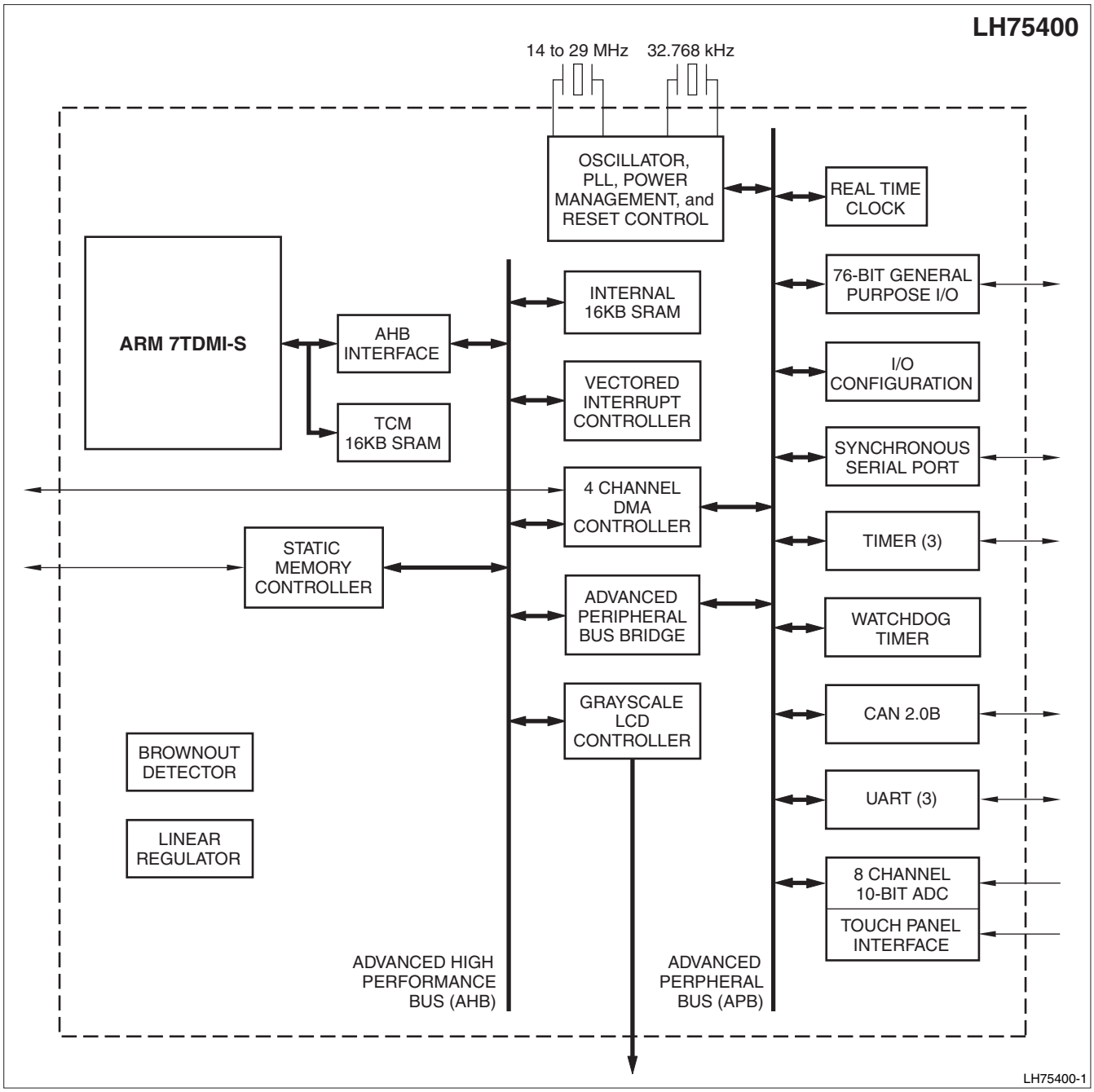


Figure 3. LH75400 Block Diagram

LH75410 BLOCK DIAGRAM

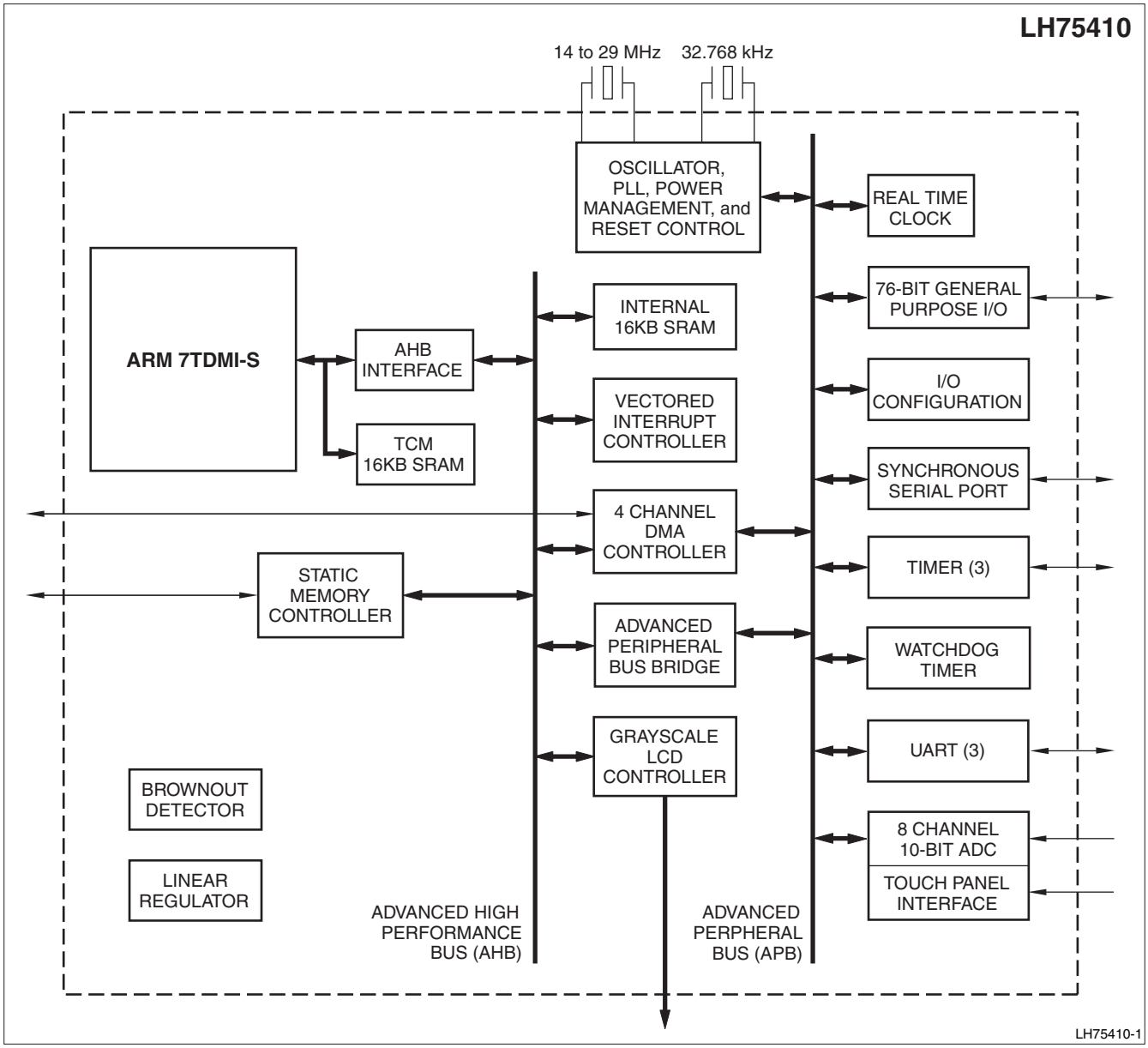


Figure 4. LH75410 Block Diagram

THE LH75401

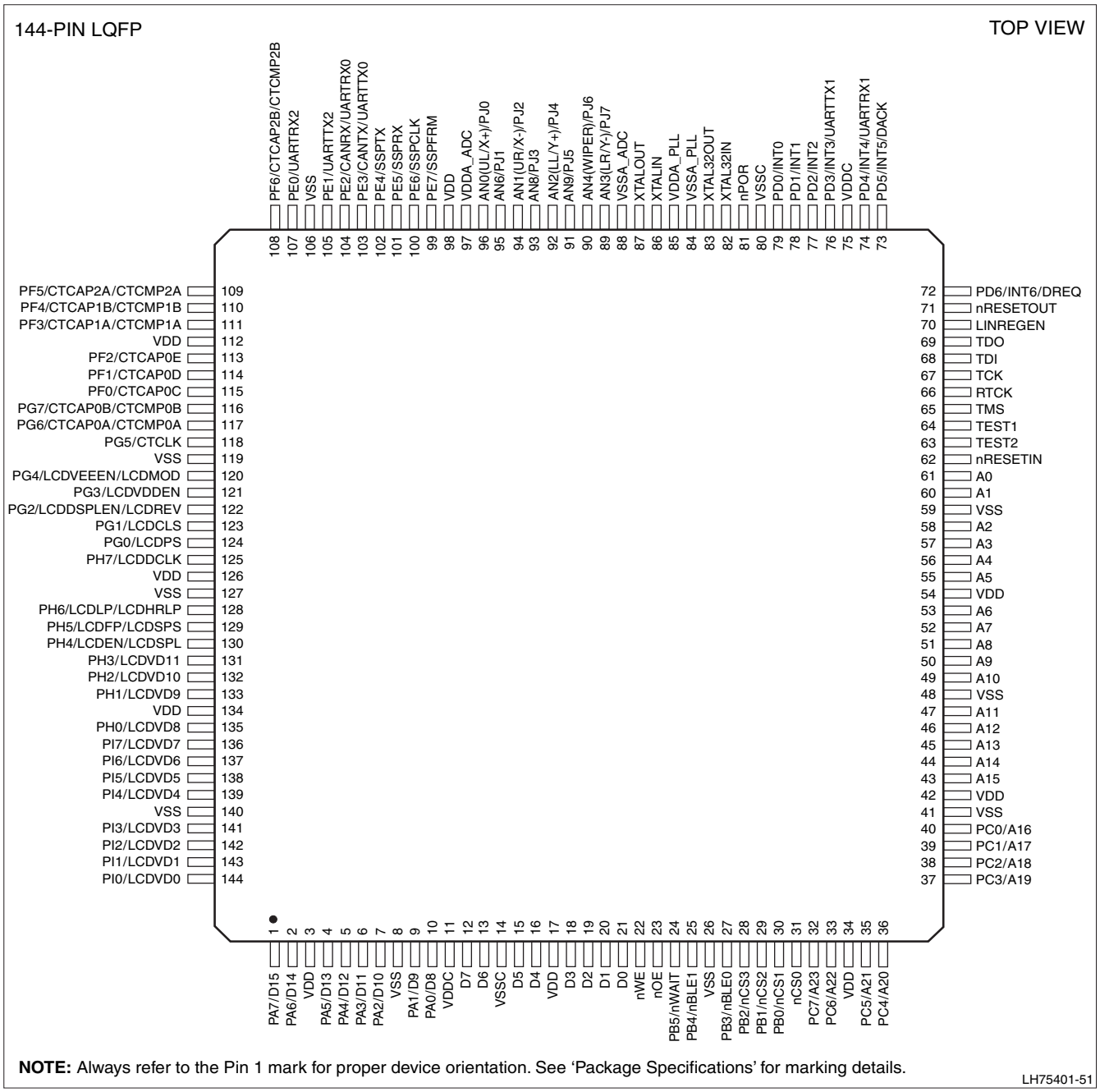


Figure 5. LH75401 Pin Diagram

LH75401 Numerical Pin Listing

Table 1. LH75401 Numerical Pin List

PIN NO.	FUNCTION AT RESET	FUNCTION 2	FUNCTION 3	FUNCTION TYPE	OUTPUT DRIVE	BUFFER TYPE	BEHAVIOR DURING RESET	NOTES
1	PA7	D15		I/O	8 mA	Bidirectional	Pull-up	1
2	PA6	D14		I/O	8 mA	Bidirectional	Pull-up	1
3	VDD			Power	None			
4	PA5	D13		I/O	8 mA	Bidirectional	Pull-up	1
5	PA4	D12		I/O	8 mA	Bidirectional	Pull-up	1
6	PA3	D11		I/O	8 mA	Bidirectional	Pull-up	1
7	PA2	D10		I/O	8 mA	Bidirectional	Pull-up	1
8	VSS			Ground	None			
9	PA1	D9		I/O	8 mA	Bidirectional	Pull-up	1
10	PA0	D8		I/O	8 mA	Bidirectional	Pull-up	1
11	VDDC			Power	None			
12	D7			I/O	8 mA	Bidirectional	Pull-up	
13	D6			I/O	8 mA	Bidirectional	Pull-up	
14	VSSC			Ground	None			
15	D5			I/O	8 mA	Bidirectional	Pull-up	
16	D4			I/O	8 mA	Bidirectional	Pull-up	
17	VDD			Power	None			
18	D3			I/O	8 mA	Bidirectional	Pull-up	
19	D2			I/O	8 mA	Bidirectional	Pull-up	
20	D1			I/O	8 mA	Bidirectional	Pull-up	
21	D0			I/O	8 mA	Bidirectional	Pull-up	
22	nWE				8 mA	Output	HIGH	3
23	nOE				8 mA	Output	HIGH	3
24	PB5	nWAIT			8 mA	Bidirectional	Pull-up	1, 3
25	PB4	nBLE1			8 mA	Bidirectional	Pull-up	1, 3
26	VSS			Ground	None			
27	PB3	nBLE0			8 mA	Bidirectional	Pull-up	1, 3
28	PB2	nCS3			8 mA	Bidirectional	Pull-up	1, 3
29	PB1	nCS2			8 mA	Bidirectional	Pull-up	1, 3
30	PB0	nCS1			8 mA	Bidirectional	Pull-up	1, 3
31	nCS0				8 mA	Output	Pull-up	3
32	PC7	A23			8 mA	Bidirectional	Pull-down	1
33	PC6	A22			8 mA	Bidirectional	Pull-down	1
34	VDD			Power	None			
35	PC5	A21			8 mA	Bidirectional	Pull-down	1
36	PC4	A20			8 mA	Bidirectional	Pull-down	1
37	PC3	A19			8 mA	Bidirectional	Pull-down	1
38	PC2	A18			8 mA	Bidirectional	Pull-down	1

Table 1. LH75401 Numerical Pin List (Cont'd)

PIN NO.	FUNCTION AT RESET	FUNCTION 2	FUNCTION 3	FUNCTION TYPE	OUTPUT DRIVE	BUFFER TYPE	BEHAVIOR DURING RESET	NOTES
39	PC1	A17			8 mA	Bidirectional	Pull-down	1
40	PC0	A16			8 mA	Bidirectional	Pull-down	1
41	VSS			Ground	None			
42	VDD			Power	None			
43	A15				8 mA	Output	LOW	
44	A14				8 mA	Output	LOW	
45	A13				8 mA	Output	LOW	
46	A12				8 mA	Output	LOW	
47	A11				8 mA	Output	LOW	
48	VSS			Ground	None			
49	A10				8 mA	Output	LOW	
50	A9				8 mA	Output	LOW	
51	A8				8 mA	Output	LOW	
52	A7				8 mA	Output	LOW	
53	A6				8 mA	Output	LOW	
54	VDD			Power	None			
55	A5				8 mA	Output	LOW	
56	A4				8 mA	Output	LOW	
57	A3				8 mA	Output	LOW	
58	A2				8 mA	Output	LOW	
59	VSS			Ground	None			
60	A1				8 mA	Output	LOW	
61	A0				8 mA	Output	LOW	
62	nRESETIN				None	Input	Pull-up	2, 3
63	TEST2				None	Input	Pull-up	2
64	TEST1				None	Input	Pull-up	2
65	TMS				None	Input	Pull-up	2
66	RTCK				4 mA	Output		
67	TCK				None	Input		
68	TDI				None	Input	Pull-up	2
69	TDO				4 mA	Output		
70	LINREGEN				None	Input		5
71	nRESETOUT				8 mA	Output		3
72	PD6	INT6	DREQ		6 mA	Bidirectional	Pull-down	1
73	PD5	INT5	DACK		6 mA	Bidirectional		1, 2
74	PD4	INT4	UARTRX1		8 mA	Bidirectional	Pull-up	1
75	VDDC			Power	None			
76	PD3	INT3	UARTTX1		8 mA	Bidirectional	Pull-up	1
77	PD2	INT2			2 mA	Bidirectional	Pull-up	1
78	PD1	INT1			6 mA	Bidirectional		1, 2
79	PD0	INT0			2 mA	Bidirectional		1
80	VSSC			Ground	None			

Table 1. LH75401 Numerical Pin List (Cont'd)

PIN NO.	FUNCTION AT RESET	FUNCTION 2	FUNCTION 3	FUNCTION TYPE	OUTPUT DRIVE	BUFFER TYPE	BEHAVIOR DURING RESET	NOTES
81	nPOR				None	Input	Pull-up	2, 3
82	XTAL32IN				None	Output		4
83	XTAL32OUT				None	Output		
84	VSSA_PLL			Ground	None			
85	VDDA_PLL			Power	None			
86	XTALIN				None	Input		4
87	XTALOUT				None	Output		
88	VSSA_ADC			Ground	None			
89	AN3 (LR/Y-)	PJ7			None	Input		
90	AN4 (Wiper)	PJ6			None	Input		
91	AN9	PJ5			None	Input		
92	AN2 (LL/Y+)	PJ4			None	Input		
93	AN8	PJ3			None	Input		
94	AN1 (UR/X-)	PJ2			None	Input		
95	AN6	PJ1			None	Input		
96	AN0 (UL/X+)	PJ0			None	Input		
97	VDDA_ADC			Power	None			
98	VDD			Power	None			
99	PE7	SSPFRM			4 mA	Bidirectional	Pull-up	1
100	PE6	SSPCLK			4 mA	Bidirectional	Pull-down	1
101	PE5	SSPRX			4 mA	Bidirectional	Pull-up	1
102	PE4	SSPTX			4 mA	Bidirectional	Pull-down	1
103	PE3	CANTX	UARTTX0		8 mA	Bidirectional	Pull-up	1
104	PE2	CANRX	UARTRX0		2 mA	Bidirectional	Pull-up	1
105	PE1	UARTTX2			4 mA	Bidirectional	Pull-up	1
106	VSS			Ground	None			
107	PE0	UARTRX2			4 mA	Bidirectional	Pull-up	1
108	PF6	CTCAP2B	CTCMP2B		4 mA	Bidirectional		2
109	PF5	CTCAP2A	CTCMP2A		4 mA	Bidirectional		
110	PF4	CTCAP1B	CACMP1B		4 mA	Bidirectional		2
111	PF3	CTCAP1A	CTCMP1A		4 mA	Bidirectional		
112	VDD			Power	None			
113	PF2	CTCAP0E			4 mA	Bidirectional		2
114	PF1	CTCAP0D			4 mA	Bidirectional		
115	PF0	CTCAP0C			4 mA	Bidirectional		2
116	PG7	CTCAP0B	CTCMP0B		4 mA	Bidirectional		
117	PG6	CTCAP0A	CTCMP0A		4 mA	Bidirectional		2
118	PG5	CTCLK			4 mA	Bidirectional		
119	VSS			Ground	None			
120	PG4	LCDVEEEN	LCDMOD		8 mA	Bidirectional		
121	PG3	LCDVDDEN			8 mA	Bidirectional		
122	PG2	LCDDSPLEN	LCDREV		8 mA	Bidirectional		

Table 1. LH75401 Numerical Pin List (Cont'd)

PIN NO.	FUNCTION AT RESET	FUNCTION 2	FUNCTION 3	FUNCTION TYPE	OUTPUT DRIVE	BUFFER TYPE	BEHAVIOR DURING RESET	NOTES
123	PG1	LCDCLS			8 mA	Bidirectional		
124	PG0	LCDPS			8 mA	Bidirectional		
125	PH7	LCDDCLK			8 mA	Bidirectional		
126	VDD			Power	None			
127	VSS			Ground	None			
128	PH6	LCDLP	LCDHRLP		8 mA	Bidirectional		
129	PH5	LCDFP	LCDSPS		8 mA	Bidirectional		
130	PH4	LCDEN	LCDSPL		8 mA	Bidirectional		
131	PH3	LCDVD11			8 mA	Bidirectional		
132	PH2	LCDVD10			8 mA	Bidirectional		
133	PH1	LCDVD9			8 mA	Bidirectional		
134	VDD			Power	None			
135	PH0	LCDVD8			8 mA	Bidirectional		
136	PI7	LCDVD7			8 mA	Bidirectional		
137	PI6	LCDVD6			8 mA	Bidirectional		
138	PI5	LCDVD5			8 mA	Bidirectional		
139	PI4	LCDVD4			8 mA	Bidirectional		
140	VSS			Ground	None			
141	PI3	LCDVD3			8 mA	Bidirectional		
142	PI2	LCDVD2			8 mA	Bidirectional		
143	PI1	LCDVD1			8 mA	Bidirectional		
144	PI0	LCDVD0			8 mA	Bidirectional		

NOTES:

1. Signal is selectable as pull-up, pull-down, or no pull-up/pull-down via the I/O Configuration peripheral.
2. CMOS Schmitt trigger input.
3. Signals preceded with 'n' are active LOW.
4. Crystal Oscillator Inputs should be driven to 1.8 V ±10% (MAX.)
5. LINREGEN activation requires a 0 Ω pull-up to VDD.

LH75401 Signal Descriptions

Table 2. LH75401 Signal Descriptions

PIN NO.	SIGNAL NAME	TYPE	DESCRIPTION	NOTES
MEMORY INTERFACE (MI)				
1 2 4 5 6 7 9 10 12 13 15 16 18 19 20 21	D[15:0]	Input/Output	Data Input/Output Signals	1
22	nWE	Output	Static Memory Controller Write Enable	2
23	nOE	Output	Static Memory Controller Output Enable	2
24	nWAIT	Input	Static Memory Controller External Wait Control	1, 2
25	nBLE1	Output	Static Memory Controller Byte Lane Strobe	1, 2
27	nBLE0	Output	Static Memory Controller Byte Lane Strobe	1, 2
28	nCS3	Output	Static Memory Controller Chip Select	1, 2
29	nCS2	Output	Static Memory Controller Chip Select	1, 2
30	nCS1	Output	Static Memory Controller Chip Select	1, 2
31	nCS0	Output	Static Memory Controller Chip Select	2
32 33 35 36 37 38 39 40 43 44 45 46 47 49 50 51 52 53 55 56 57 58 60 61	A[23:0]	Output	Address Signals	1
DMA CONTROLLER (DMAC)				
72	DREQ	Input	DMA Request	1
73	DACK	Output	DMA Acknowledge	1

Table 2. LH75401 Signal Descriptions (Cont'd)

PIN NO.	SIGNAL NAME	TYPE	DESCRIPTION	NOTES
COLOR LCD CONTROLLER (CLCDC)				
120	LCDMOD	Output	Signal Used by the Row Driver (AD-TFT, HR-TFT only)	1
120	LCDVEEEN	Output	Analog Supply Enable (AC Bias SIgnal)	1
121	LCDVDDEN	Output	Digital Supply Enable	1
122	LCDDSPLEN	Output	LCD Panel Power Enable	1
122	LCDREV	Output	Reverse Signal (AD-TFT, HR-TFT only)	1
123	LCDCLS	Output	Clock to the Row Drivers (AD-TFT, HR-TFT only)	1
124	LCDPS	Output	Power Save (AD-TFT, HR-TFT only)	1
125	LCDDCLK	Output	LCD Panel Clock	1
128	LCDLP	Output	Line Synchronization Pulse (STN), Horizontal Synchronization Pulse (TFT)	1
128	LCDHRLP	Output	Latch Pulse (AD-TFT, HR-TFT only)	1
129	LCDFP	Output	Frame Pulse (STN), Vertical Synchronization Pulse (TFT)	1
129	LCDSPS	Output	Row Driver Counter Reset Signal (AD-TFT, HR-TFT only)	1
130	LCDEN	Output	LCD Data Enable	1
130	LCDSPL	Output	Start Pulse Left (AD-TFT, HR-TFT only)	1
131 132 133 135 136 137 138 139 141 142 143 144	LCDVD[11:0]	Output	LCD Panel Data bus	1
SYNCHRONOUS SERIAL PORT (SSP)				
99	SSPFRM	Output	SSP Serial Frame	1
100	SSPCLK	Output	SSP Clock	1
101	SSPRX	Input	SSP RXD	1
102	SSPTX	Output	SSP TXD	1
UART0 (U0)				
103	UARTTX0	Output	UART0 Transmitted Serial Data Output	1
104	UARTRX0	Input	UART0 Received Serial Data Input	1
UART1 (U1)				
74	UARTRX1	Input	UART1 Received Serial Data Input	1
76	UARTTX1	Output	UART1 Transmitted Serial Data Output	1
UART2 (U2)				
105	UARTTX2	Output	UART2 Transmitted Serial Data Output	1
107	UARTRX2	Input	UART2 Received Serial Data Input	1
CONTROLLER AREA NETWORK (CAN)				
103	CANTX	Output	CAN Transmitted Serial Data Output	1
104	CANRX	Input	CAN Received Serial Data Input	1

Table 2. LH75401 Signal Descriptions (Cont'd)

PIN NO.	SIGNAL NAME	TYPE	DESCRIPTION	NOTES
ANALOG-TO-DIGITAL CONVERTER (ADC)				
89 90 91 92 93 94 95 96	AN3 (LR/Y-) AN4 (Wiper) AN9 AN2 (LL/Y+) AN8 AN1 (UR/X-) AN6 AN0 (UL/X+)	Input	ADC Inputs	1
TIMER 0				
117 116 115 114 113	CTCAP0[A:E]	Input	Timer 0 Capture Inputs	1
117 116	CTCMP0[A:B]	Output	Timer 0 Compare Outputs	1
118	CTCLK	Input	Common External Clock	1
TIMER 1				
111 110	CTCAP1[A:B]	Input	Timer 1 Capture Inputs	1
111 110	CTCMP1[A:B]	Output	Timer 1 Compare Outputs	1
118	CTCLK	Input	Common External Clock	1
TIMER 2				
109 108	CTCAP2[A:B]	Input	Timer 2 Capture Inputs	1
109 108	CTCMP2[A:B]	Input	Timer 2 Compare Outputs	1
118	CTCLK	Input	Common External Clock	1
GENERAL PURPOSE INPUT/OUTPUT (GPIO)				
1 2 4 5 6 7 9 10	PA7 PA6 PA5 PA4 PA3 PA2 PA1 PA0	Input/Output	General Purpose I/O Signals - Port A	1
24 25 27 28 29 30	PB5 PB4 PB3 PB2 PB1 PB0	Input/Output	General Purpose I/O Signals - Port B	1
32 33 35 36 37 38 39 40	PC7 PC6 PC5 PC4 PC3 PC2 PC1 PC0	Input/Output	General Purpose I/O Signals - Port C	1

Table 2. LH75401 Signal Descriptions (Cont'd)

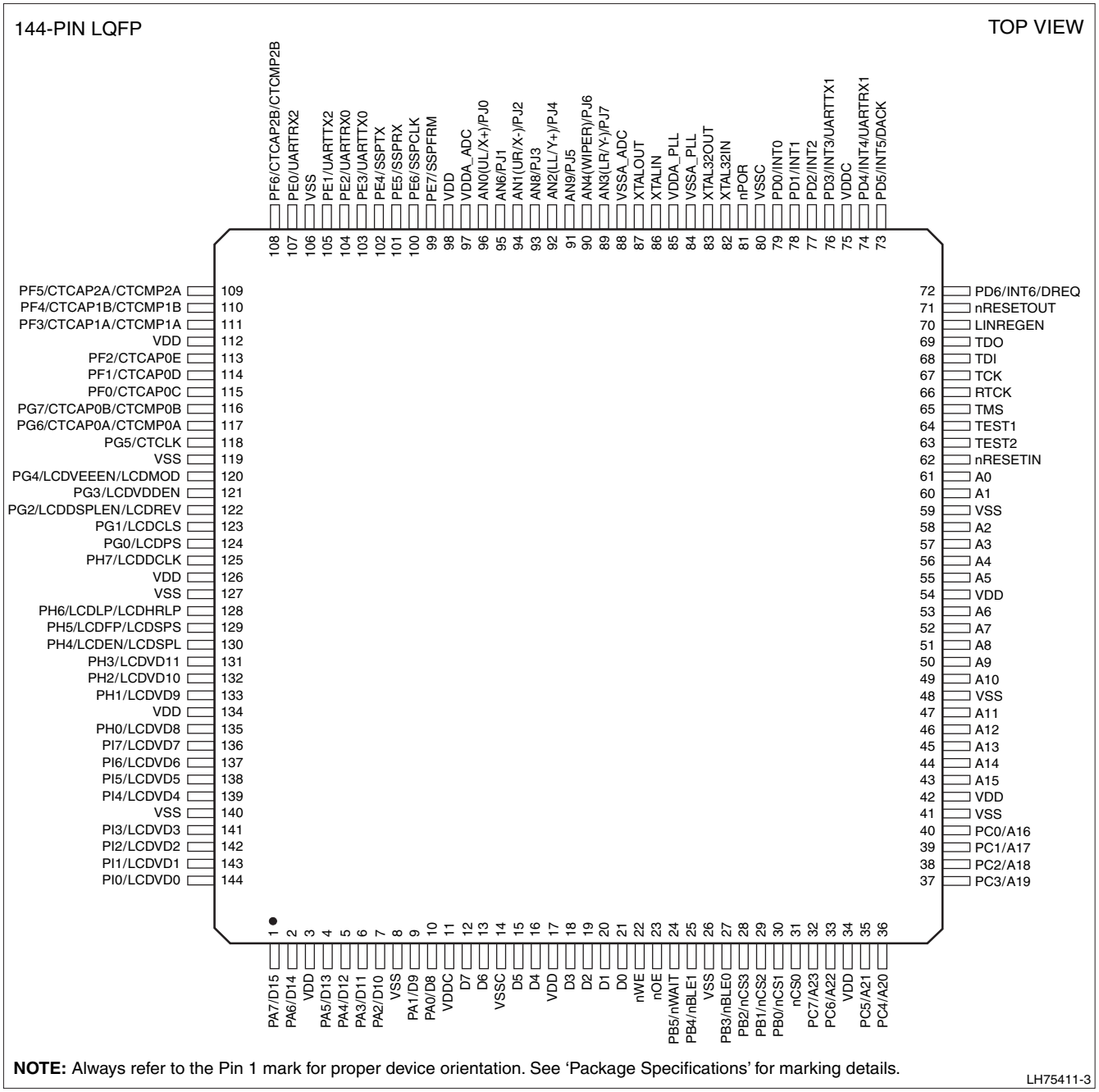
PIN NO.	SIGNAL NAME	TYPE	DESCRIPTION	NOTES
72 73 74 76 77 78 79	PD6 PD5 PD4 PD3 PD2 PD1 PD0	Input/Output	General Purpose I/O Signals - Port D	1
89 90 91 92 93 94 95 96	PJ7 PJ6 PJ5 PJ4 PJ3 PJ2 PJ1 PJ0	Input	General Purpose I/O Signals - Port J	1
99 100 101 102 103 104 105 107	PE7 PE6 PE5 PE4 PE3 PE2 PE1 PE0	Input/Output	General Purpose I/O Signals - Port E	1
108 109 110 111 113 114 115	PF6 PF5 PF4 PF3 PF2 PF1 PF0	Input/Output	General Purpose I/O Signals - Port F	1
116 117 118 120 121 122 123 124	PG7 PG6 PG5 PG4 PG3 PG2 PG1 PG0	Input/Output	General Purpose I/O Signals - Port G	1
125 128 129 130 131 132 133 135	PH7 PH6 PH5 PH4 PH3 PH2 PH1 PH0	Input/Output	General Purpose I/O Signals - Port H	1
136 137 138 139 141 142 143 144	PI7 PI6 PI5 PI4 PI3 PI2 PI1 PI0	Input/Output	General Purpose I/O Signals - Port I	1
RESET, CLOCK, AND POWER CONTROLLER (RCPC)				
62	nRESETIN	Input	User Reset Input	2
71	nRESETOUT	Output	System Reset Output	2
72	INT6	Input	External Interrupt Input 6	1

Table 2. LH75401 Signal Descriptions (Cont'd)

PIN NO.	SIGNAL NAME	TYPE	DESCRIPTION	NOTES
73	INT5	Input	External Interrupt Input 5	1
74	INT4	Input	External Interrupt Input 4	1
76	INT3	Input	External Interrupt Input 3	1
77	INT2	Input	External Interrupt Input 2	1
78	INT1	Input	External Interrupt Input 1	1
79	INT0	Input	External Interrupt Input 0	1
81	nPOR	Input	Power-on Reset Input	2
82	XTAL32IN	Input	32.768 kHz Crystal Clock Input	
83	XTAL32OUT	Output	32.768 kHz Crystal Clock Output	
86	XTALIN	Input	Crystal Clock Input	
87	XTALOUT	Output	Crystal Clock Output	
TEST INTERFACE				
63	TEST2	Input	Test Mode Pin 2	
64	TEST1	Input	Test Mode Pin 1	
65	TMS	Input	JTAG Test Mode Select Input	
66	RTCK	Output	Returned JTAG Test Clock Output	
67	TCK	Input	JTAG Test Clock Input	
68	TDI	Input	JTAG Test Serial Data Input	
69	TDO	Output	JTAG Test Data Serial Output	
POWER AND GROUND (GND)				
3 17 34 42 54 98 112 126 134	VDD	Power	I/O Ring VDD	
8 26 41 48 59 106 119 127 140	VSS	Power	I/O Ring VSS	
11 75	VDDC	Power	Core VDD supply (Output if Linear Regulator Enabled, Otherwise Input)	
14 80	VSSC	Power	Core VSS	
70	LINREGEN	Input	Linear Regulator Enable	
84	VSSA_PLL	Power	PLL Analog VSS	
85	VDDA_PLL	Power	PLL Analog VDD Supply	
88	VSSA_ADC	Power	A-to-D converter Analog VSS	
97	VDDA_ADC	Power	A-to-D converter Analog VDD Supply	

NOTES:
1. These pin numbers have multiplexed functions.
2. Signals preceded with 'n' are active LOW.

THE LH75411



NOTE: Always refer to the Pin 1 mark for proper device orientation. See 'Package Specifications' for marking details.

Figure 6. LH75411 Pin Diagram

LH75411 Numerical Pin Listing

Table 3. LH75411 Numerical Pin List

PIN NO.	FUNCTION AT RESET	FUNCTION 2	FUNCTION 3	FUNCTION TYPE	OUTPUT DRIVE	BUFFER TYPE	BEHAVIOR DURING RESET	NOTES
1	PA7	D15		I/O	8 mA	Bidirectional	Pull-up	1
2	PA6	D14		I/O	8 mA	Bidirectional	Pull-up	1
3	VDD			Power	None			
4	PA5	D13		I/O	8 mA	Bidirectional	Pull-up	1
5	PA4	D12		I/O	8 mA	Bidirectional	Pull-up	1
6	PA3	D11		I/O	8 mA	Bidirectional	Pull-up	1
7	PA2	D10		I/O	8 mA	Bidirectional	Pull-up	1
8	VSS			Ground	None			
9	PA1	D9		I/O	8 mA	Bidirectional	Pull-up	1
10	PA0	D8		I/O	8 mA	Bidirectional	Pull-up	1
11	VDDC			Power	None			
12	D7			I/O	8 mA	Bidirectional	Pull-up	
13	D6			I/O	8 mA	Bidirectional	Pull-up	
14	VSSC			Ground	None			
15	D5			I/O	8 mA	Bidirectional	Pull-up	
16	D4			I/O	8 mA	Bidirectional	Pull-up	
17	VDD			Power	None			
18	D3			I/O	8 mA	Bidirectional	Pull-up	
19	D2			I/O	8 mA	Bidirectional	Pull-up	
20	D1			I/O	8 mA	Bidirectional	Pull-up	
21	D0			I/O	8 mA	Bidirectional	Pull-up	
22	nWE				8 mA	Output	HIGH	3
23	nOE				8 mA	Output	HIGH	3
24	PB5	nWAIT			8 mA	Bidirectional	Pull-up	1, 3
25	PB4	nBLE1			8 mA	Bidirectional	Pull-up	1, 3
26	VSS			Ground	None			
27	PB3	nBLE0			8 mA	Bidirectional	Pull-up	1, 3
28	PB2	nCS3			8 mA	Bidirectional	Pull-up	1, 3
29	PB1	nCS2			8 mA	Bidirectional	Pull-up	1, 3
30	PB0	nCS1			8 mA	Bidirectional	Pull-up	1, 3
31	nCS0				8 mA	Output	Pull-up	3
32	PC7	A23			8 mA	Bidirectional	Pull-down	1
33	PC6	A22			8 mA	Bidirectional	Pull-down	1
34	VDD			Power	None			
35	PC5	A21			8 mA	Bidirectional	Pull-down	1
36	PC4	A20			8 mA	Bidirectional	Pull-down	1
37	PC3	A19			8 mA	Bidirectional	Pull-down	1
38	PC2	A18			8 mA	Bidirectional	Pull-down	1
39	PC1	A17			8 mA	Bidirectional	Pull-down	1
40	PC0	A16			8 mA	Bidirectional	Pull-down	1
41	VSS			Ground	None			

Table 3. LH75411 Numerical Pin List (Cont'd)

PIN NO.	FUNCTION AT RESET	FUNCTION 2	FUNCTION 3	FUNCTION TYPE	OUTPUT DRIVE	BUFFER TYPE	BEHAVIOR DURING RESET	NOTES
42	VDD			Power	None			
43	A15				8 mA	Output	LOW	
44	A14				8 mA	Output	LOW	
45	A13				8 mA	Output	LOW	
46	A12				8 mA	Output	LOW	
47	A11				8 mA	Output	LOW	
48	VSS			Ground	None			
49	A10				8 mA	Output	LOW	
50	A9				8 mA	Output	LOW	
51	A8				8 mA	Output	LOW	
52	A7				8 mA	Output	LOW	
53	A6				8 mA	Output	LOW	
54	VDD			Power	None			
55	A5				8 mA	Output	LOW	
56	A4				8 mA	Output	LOW	
57	A3				8 mA	Output	LOW	
58	A2				8 mA	Output	LOW	
59	VSS			Ground	None			
60	A1				8 mA	Output	LOW	
61	A0				8 mA	Output	LOW	
62	nRESETIN				None	Input	Pull-up	2, 3
63	TEST2				None	Input	Pull-up	2
64	TEST1				None	Input	Pull-up	2
65	TMS				None	Input	Pull-up	2
66	RTCK				4 mA	Output		
67	TCK				None	Input		
68	TDI				None	Input	Pull-up	2
69	TDO				4 mA	Output		
70	LINREGEN				None	Input		5
71	nRESETOUT				8 mA	Output		3
72	PD6	INT6	DREQ		6 mA	Bidirectional	Pull-down	1
73	PD5	INT5	DACK		6 mA	Bidirectional		1, 2
74	PD4	INT4	UARTRX1		8 mA	Bidirectional	Pull-up	1
75	VDDC			Power	None			
76	PD3	INT3	UARTTX1		8 mA	Bidirectional	Pull-up	1
77	PD2	INT2			2 mA	Bidirectional	Pull-up	1
78	PD1	INT1			6 mA	Bidirectional		1, 2
79	PD0	INT0			2 mA	Bidirectional		1
80	VSSC			Ground	None			
81	nPOR				None	Input	Pull-up	2, 3
82	XTAL32IN				None	Output		4
83	XTAL32OUT				None	Output		

Table 3. LH75411 Numerical Pin List (Cont'd)

PIN NO.	FUNCTION AT RESET	FUNCTION 2	FUNCTION 3	FUNCTION TYPE	OUTPUT DRIVE	BUFFER TYPE	BEHAVIOR DURING RESET	NOTES
84	VSSA_PLL			Ground	None			
85	VDDA_PLL			Power	None			
86	XTALIN				None	Input		4
87	XTALOUT				None	Output		
88	VSSA_ADC			Ground	None			
89	AN3 (LR/Y-)	PJ7			None	Input		
90	AN4 (Wiper)	PJ6			None	Input		
91	AN9	PJ5			None	Input		
92	AN2 (LL/Y+)	PJ4			None	Input		
93	AN8	PJ3			None	Input		
94	AN1 (UR/X-)	PJ2			None	Input		
95	AN6	PJ1			None	Input		
96	AN0 (UL/X+)	PJ0			None	Input		
97	VDDA_ADC			Power	None			
98	VDD			Power	None			
99	PE7	SSPFRM			4 mA	Bidirectional	Pull-up	1
100	PE6	SSPCLK			4 mA	Bidirectional	Pull-down	1
101	PE5	SSPRX			4 mA	Bidirectional	Pull-up	1
102	PE4	SSPTX			4 mA	Bidirectional	Pull-down	1
103	PE3	UARTTX0			8 mA	Bidirectional	Pull-up	1
104	PE2	UARTRX0			2 mA	Bidirectional	Pull-up	1
105	PE1	UARTTX2			4 mA	Bidirectional	Pull-up	1
106	VSS			Ground	None			
107	PE0	UARTRX2			4 mA	Bidirectional	Pull-up	1
108	PF6	CTCAP2B	CTCMP2B		4 mA	Bidirectional		2
109	PF5	CTCAP2A	CTCMP2A		4 mA	Bidirectional		
110	PF4	CTCAP1B	CACMP1B		4 mA	Bidirectional		2
111	PF3	CTCAP1A	CTCMP1A		4 mA	Bidirectional		
112	VDD			Power	None			
113	PF2	CTCAP0E			4 mA	Bidirectional		2
114	PF1	CTCAP0D			4 mA	Bidirectional		
115	PF0	CTCAP0C			4 mA	Bidirectional		2
116	PG7	CTCAP0B	CTCMP0B		4 mA	Bidirectional		
117	PG6	CTCAP0A	CTCMP0A		4 mA	Bidirectional		2
118	PG5	CTCLK			4 mA	Bidirectional		
119	VSS			Ground	None			
120	PG4	LCDVEEEN	LCDMOD		8 mA	Bidirectional		
121	PG3	LCDVDDEN			8 mA	Bidirectional		
122	PG2	LCDDSPLEN	LCDREV		8 mA	Bidirectional		
123	PG1	LCDCLS			8 mA	Bidirectional		
124	PG0	LCDPS			8 mA	Bidirectional		
125	PH7	LCDDCLK			8 mA	Bidirectional		

Table 3. LH75411 Numerical Pin List (Cont'd)

PIN NO.	FUNCTION AT RESET	FUNCTION 2	FUNCTION 3	FUNCTION TYPE	OUTPUT DRIVE	BUFFER TYPE	BEHAVIOR DURING RESET	NOTES
126	VDD			Power	None			
127	VSS			Ground	None			
128	PH6	LCDLP	LCDHRLP		8 mA	Bidirectional		
129	PH5	LCDFP	LCDSPS		8 mA	Bidirectional		
130	PH4	LCDEN	LCDSPL		8 mA	Bidirectional		
131	PH3	LCDVD11			8 mA	Bidirectional		
132	PH2	LCDVD10			8 mA	Bidirectional		
133	PH1	LCDVD9			8 mA	Bidirectional		
134	VDD			Power	None			
135	PH0	LCDVD8			8 mA	Bidirectional		
136	PI7	LCDVD7			8 mA	Bidirectional		
137	PI6	LCDVD6			8 mA	Bidirectional		
138	PI5	LCDVD5			8 mA	Bidirectional		
139	PI4	LCDVD4			8 mA	Bidirectional		
140	VSS			Ground	None			
141	PI3	LCDVD3			8 mA	Bidirectional		
142	PI2	LCDVD2			8 mA	Bidirectional		
143	PI1	LCDVD1			8 mA	Bidirectional		
144	PI0	LCDVD0			8 mA	Bidirectional		

NOTES:

1. Signal is selectable as pull-up, pull-down, or no pull-up/pull-down via the I/O Configuration peripheral.
2. CMOS Schmitt trigger input.
3. Signals preceded with 'n' are active LOW.
4. Crystal Oscillator Inputs should be driven to 1.8 V ±10% (MAX.)
5. LINREGEN activation requires a 0 Ω pull-up to VDD.

LH75411 Signal Descriptions

Table 4. LH75411 Signal Descriptions

PIN NO.	SIGNAL NAME	TYPE	DESCRIPTION	NOTES
MEMORY INTERFACE (MI)				
1 2 4 5 6 7 9 10 12 13 15 16 18 19 20 21	D[15:0]	Input/Output	Data Input/Output Signals	1
22	nWE	Output	Static Memory Controller Write Enable	2
23	nOE	Output	Static Memory Controller Output Enable	2
24	nWAIT	Input	Static Memory Controller External Wait Control	1, 2
25	nBLE1	Output	Static Memory Controller Byte Lane Strobe	1, 2
27	nBLE0	Output	Static Memory Controller Byte Lane Strobe	1, 2
28	nCS3	Output	Static Memory Controller Chip Select	1, 2
29	nCS2	Output	Static Memory Controller Chip Select	1, 2
30	nCS1	Output	Static Memory Controller Chip Select	1, 2
31	nCS0	Output	Static Memory Controller Chip Select	2
32 33 35 36 37 38 39 40 43 44 45 46 47 49 50 51 52 53 55 56 57 58 60 61	A[23:0]	Output	Address Signals	1
DMA CONTROLLER (DMAC)				
72	DREQ	Input	DMA Request	1
73	DACK	Output	DMA Acknowledge	1

Table 4. LH75411 Signal Descriptions (Cont'd)

PIN NO.	SIGNAL NAME	TYPE	DESCRIPTION	NOTES
COLOR LCD CONTROLLER (CLCDC)				
120	LCDMOD	Output	Signal Used by the Row Driver (AD-TFT, HR-TFT only)	1
120	LCDVEEEN	Output	Analog Supply Enable (AC Bias SIgnal)	1
121	LCDVDDEN	Output	Digital Supply Enable	1
122	LCDDSPLEN	Output	LCD Panel Power Enable	1
122	LCDREV	Output	Reverse Signal (AD-TFT, HR-TFT only)	1
123	LCDCLS	Output	Clock to the Row Drivers (AD-TFT, HR-TFT only)	1
124	LCDPS	Output	Power Save (AD-TFT, HR-TFT only)	1
125	LCDDCLK	Output	LCD Panel Clock	1
128	LCDLP	Output	Line Synchronization Pulse (STN), Horizontal Synchronization Pulse (TFT)	1
128	LCDHRLP	Output	Latch Pulse (AD-TFT, HR-TFT only)	1
129	LCDFP	Output	Frame Pulse (STN), Vertical Synchronization Pulse (TFT)	1
129	LCDSPS	Output	Row Driver Counter Reset Signal (AD-TFT, HR-TFT only)	1
130	LCDEN	Output	LCD Data Enable	1
130	LCDSPL	Output	Start Pulse Left (AD-TFT, HR-TFT only)	1
131 132 133 135 136 137 138 139 141 142 143 144	LCDVD[11:0]	Output	LCD Panel Data bus	1
SYNCHRONOUS SERIAL PORT (SSP)				
99	SSPFRM	Output	SSP Serial Frame	1
100	SSPCLK	Output	SSP Clock	1
101	SSPRX	Input	SSP RXD	1
102	SSPTX	Output	SSP TXD	1
UART0 (U0)				
104	UARTRX0	Input	UART0 Received Serial Data Input	1
103	UARTTX0	Output	UART0 Transmitted Serial Data Output	1
UART1 (U1)				
74	UARTRX1	Input	UART1 Received Serial Data Input	1
76	UARTTX1	Output	UART1 Transmitted Serial Data Output	1
UART2 (U2)				
105	UARTTX2	Output	UART2 Transmitted Serial Data Output	1
107	UARTRX2	Input	UART2 Received Serial Data Input	1
ANALOG-TO-DIGITAL CONVERTER (ADC)				
89 90 91 92 93 94 95 96	AN3 (LR/Y-) AN4 (Wiper) AN9 AN2 (LL/Y+) AN8 AN1 (UR/X-) AN6 AN0 (UL/X+)	Input	ADC Inputs	1

Table 4. LH75411 Signal Descriptions (Cont'd)

PIN NO.	SIGNAL NAME	TYPE	DESCRIPTION	NOTES
TIMER 0				
117 116 115 114 113	CTCAP0[A:E]	Input	Timer 0 Capture Inputs	1
117 116	CTCMP0[A:B]	Output	Timer 0 Compare Outputs	1
118	CTCLK	Input	Common External Clock	1
TIMER 1				
111 110	CTCAP1[A:B]	Input	Timer 1 Capture Inputs	1
111 110	CTCMP1[A:B]	Output	Timer 1 Compare Outputs	1
118	CTCLK	Input	Common External Clock	1
TIMER 2				
109 108	CTCAP2[A:B]	Input	Timer 2 Capture Inputs	1
109 108	CTCMP2[A:B]	Input	Timer 2 Compare Outputs	1
118	CTCLK	Input	Common External Clock	1
GENERAL PURPOSE INPUT/OUTPUT (GPIO)				
1 2 4 5 6 7 9 10	PA7 PA6 PA5 PA4 PA3 PA2 PA1 PA0	Input/Output	General Purpose I/O Signals - Port A	1
24 25 27 28 29 30	PB5 PB4 PB3 PB2 PB1 PB0	Input/Output	General Purpose I/O Signals - Port B	1
32 33 35 36 37 38 39 40	PC7 PC6 PC5 PC4 PC3 PC2 PC1 PC0	Input/Output	General Purpose I/O Signals - Port C	1
72 73 74 76 77 78 79	PD6 PD5 PD4 PD3 PD2 PD1 PD0	Input/Output	General Purpose I/O Signals - Port D	1

Table 4. LH75411 Signal Descriptions (Cont'd)

PIN NO.	SIGNAL NAME	TYPE	DESCRIPTION	NOTES
89 90 91 92 93 94 95 96	PJ7 PJ6 PJ5 PJ4 PJ3 PJ2 PJ1 PJ0	Input	General Purpose I/O Signals - Port J	1
99 100 101 102 103 104 105 107	PE7 PE6 PE5 PE4 PE3 PE2 PE1 PE0	Input/Output	General Purpose I/O Signals - Port E	1
108 109 110 111 113 114 115	PF6 PF5 PF4 PF3 PF2 PF1 PF0	Input/Output	General Purpose I/O Signals - Port F	1
116 117 118 120 121 122 123 124	PG7 PG6 PG5 PG4 PG3 PG2 PG1 PG0	Input/Output	General Purpose I/O Signals - Port G	1
125 128 129 130 131 132 133 135	PH7 PH6 PH5 PH4 PH3 PH2 PH1 PH0	Input/Output	General Purpose I/O Signals - Port H	1
136 137 138 139 141 142 143 144	PI7 PI6 PI5 PI4 PI3 PI2 PI1 PI0	Input/Output	General Purpose I/O Signals - Port I	1
RESET, CLOCK, AND POWER CONTROLLER (RCPC)				
62	nRESETIN	Input	User Reset Input	2
71	nRESETOUT	Output	System Reset Output	2
72	INT6	Input	External Interrupt Input 6	1
73	INT5	Input	External Interrupt Input 5	1
74	INT4	Input	External Interrupt Input 4	1
76	INT3	Input	External Interrupt Input 3	1
77	INT2	Input	External Interrupt Input 2	1
78	INT1	Input	External Interrupt Input 1	1
79	INT0	Input	External Interrupt Input 0	1

Table 4. LH75411 Signal Descriptions (Cont'd)

PIN NO.	SIGNAL NAME	TYPE	DESCRIPTION	NOTES
81	nPOR	Input	Power-on Reset Input	2
82	XTAL32IN	Input	32.768 kHz Crystal Clock Input	
83	XTAL32OUT	Output	32.768 kHz Crystal Clock Output	
86	XTALIN	Input	Crystal Clock Input	
87	XTALOUT	Output	Crystal Clock Output	
TEST INTERFACE				
63	TEST2	Input	Test Mode Pin 2	
64	TEST1	Input	Test Mode Pin 1	
65	TMS	Input	JTAG Test Mode Select Input	
66	RTCK	Output	Returned JTAG Test Clock Output	
67	TCK	Input	JTAG Test Clock Input	
68	TDI	Input	JTAG Test Serial Data Input	
69	TDO	Output	JTAG Test Data Serial Output	
POWER AND GROUND (GND)				
3 17 34 42 54 98 112 126 134	VDD	Power	I/O Ring VDD	
8 26 41 48 59 106 119 127 140	VSS	Power	I/O Ring VSS	
11 75	VDDC	Power	Core VDD supply (Output if Linear Regulator Enabled, Otherwise Input)	
14 80	VSSC	Power	Core VSS	
70	LINREGEN	Input	Linear Regulator Enable	
84	VSSA_PLL	Power	PLL Analog VSS	
85	VDDA_PLL	Power	PLL Analog VDD Supply	
88	VSSA_ADC	Power	A-to-D converter Analog VSS	
97	VDDA_ADC	Power	A-to-D converter Analog VDD Supply	

NOTES:
1. These pin numbers have multiplexed functions.
2. Signals preceded with 'n' are active LOW.

THE LH75400

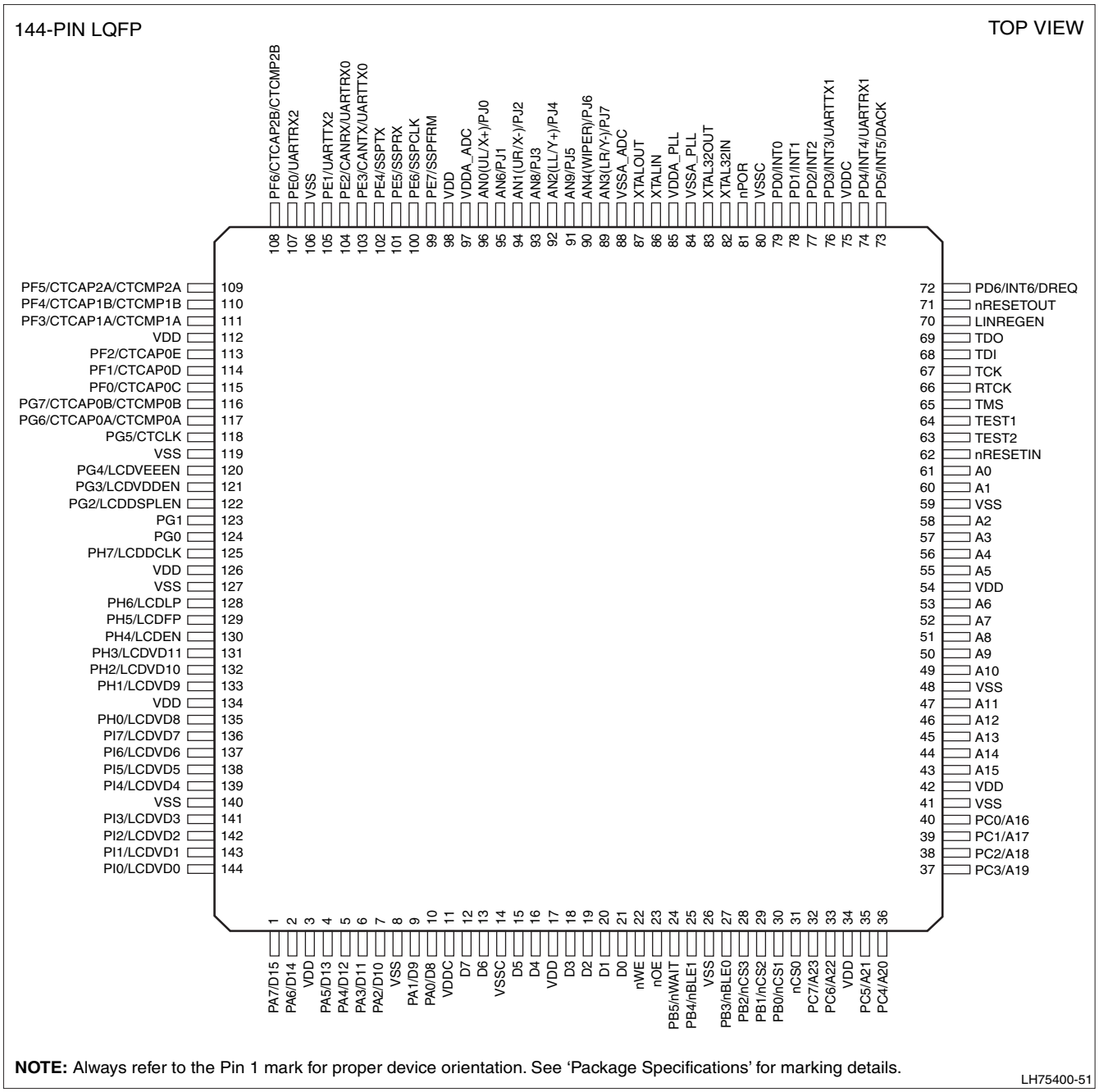


Figure 7. LH75400 Pin Diagram

LH75400 Numerical Pin Listing

Table 5. LH75400 Numerical Pin List

PIN NO.	FUNCTION AT RESET	FUNCTION 2	FUNCTION 3	FUNCTION TYPE	OUTPUT DRIVE	BUFFER TYPE	BEHAVIOR DURING RESET	NOTES
1	PA7	D15		I/O	8 mA	Bidirectional	Pull-up	1
2	PA6	D14		I/O	8 mA	Bidirectional	Pull-up	1
3	VDD			Power	None			
4	PA5	D13		I/O	8 mA	Bidirectional	Pull-up	1
5	PA4	D12		I/O	8 mA	Bidirectional	Pull-up	1
6	PA3	D11		I/O	8 mA	Bidirectional	Pull-up	1
7	PA2	D10		I/O	8 mA	Bidirectional	Pull-up	1
8	VSS			Ground	None			
9	PA1	D9		I/O	8 mA	Bidirectional	Pull-up	1
10	PA0	D8		I/O	8 mA	Bidirectional	Pull-up	1
11	VDDC			Power	None			
12	D7			I/O	8 mA	Bidirectional	Pull-up	
13	D6			I/O	8 mA	Bidirectional	Pull-up	
14	VSSC			Ground	None			
15	D5			I/O	8 mA	Bidirectional	Pull-up	
16	D4			I/O	8 mA	Bidirectional	Pull-up	
17	VDD			Power	None			
18	D3			I/O	8 mA	Bidirectional	Pull-up	
19	D2			I/O	8 mA	Bidirectional	Pull-up	
20	D1			I/O	8 mA	Bidirectional	Pull-up	
21	D0			I/O	8 mA	Bidirectional	Pull-up	
22	nWE				8 mA	Output	HIGH	3
23	nOE				8 mA	Output	HIGH	3
24	PB5	nWAIT			8 mA	Bidirectional	Pull-up	1, 3
25	PB4	nBLE1			8 mA	Bidirectional	Pull-up	1, 3
26	VSS			Ground	None			
27	PB3	nBLE0			8 mA	Bidirectional	Pull-up	1, 3
28	PB2	nCS3			8 mA	Bidirectional	Pull-up	1, 3
29	PB1	nCS2			8 mA	Bidirectional	Pull-up	1, 3
30	PB0	nCS1			8 mA	Bidirectional	Pull-up	1, 3
31	nCS0				8 mA	Output	Pull-up	3
32	PC7	A23			8 mA	Bidirectional	Pull-down	1
33	PC6	A22			8 mA	Bidirectional	Pull-down	1
34	VDD			Power	None			
35	PC5	A21			8 mA	Bidirectional	Pull-down	1
36	PC4	A20			8 mA	Bidirectional	Pull-down	1
37	PC3	A19			8 mA	Bidirectional	Pull-down	1
38	PC2	A18			8 mA	Bidirectional	Pull-down	1
39	PC1	A17			8 mA	Bidirectional	Pull-down	1
40	PC0	A16			8 mA	Bidirectional	Pull-down	1

Table 5. LH75400 Numerical Pin List (Cont'd)

PIN NO.	FUNCTION AT RESET	FUNCTION 2	FUNCTION 3	FUNCTION TYPE	OUTPUT DRIVE	BUFFER TYPE	BEHAVIOR DURING RESET	NOTES
41	VSS			Ground	None			
42	VDD			Power	None			
43	A15				8 mA	Output	LOW	
44	A14				8 mA	Output	LOW	
45	A13				8 mA	Output	LOW	
46	A12				8 mA	Output	LOW	
47	A11				8 mA	Output	LOW	
48	VSS			Ground	None			
49	A10				8 mA	Output	LOW	
50	A9				8 mA	Output	LOW	
51	A8				8 mA	Output	LOW	
52	A7				8 mA	Output	LOW	
53	A6				8 mA	Output	LOW	
54	VDD			Power	None			
55	A5				8 mA	Output	LOW	
56	A4				8 mA	Output	LOW	
57	A3				8 mA	Output	LOW	
58	A2				8 mA	Output	LOW	
59	VSS			Ground	None			
60	A1				8 mA	Output	LOW	
61	A0				8 mA	Output	LOW	
62	nRESETIN				None	Input	Pull-up	2, 3
63	TEST2				None	Input	Pull-up	2
64	TEST1				None	Input	Pull-up	2
65	TMS				None	Input	Pull-up	2
66	RTCK				4 mA	Output		
67	TCK				None	Input		
68	TDI				None	Input	Pull-up	2
69	TDO				4 mA	Output		
70	LINREGEN				None	Input		5
71	nRESETOUT				8 mA	Output		3
72	PD6	INT6	DREQ		6 mA	Bidirectional	Pull-down	1
73	PD5	INT5	DACK		6 mA	Bidirectional		1, 2
74	PD4	INT4	UARTRX1		8 mA	Bidirectional	Pull-up	1
75	VDDC			Power	None			
76	PD3	INT3	UARTTX1		8 mA	Bidirectional	Pull-up	1
77	PD2	INT2			2 mA	Bidirectional	Pull-up	1
78	PD1	INT1			6 mA	Bidirectional		1, 2
79	PD0	INT0			2 mA	Bidirectional		1
80	VSSC			Ground	None			
81	nPOR				None	Input	Pull-up	2, 3
82	XTAL32IN				None	Output		4

Table 5. LH75400 Numerical Pin List (Cont'd)

PIN NO.	FUNCTION AT RESET	FUNCTION 2	FUNCTION 3	FUNCTION TYPE	OUTPUT DRIVE	BUFFER TYPE	BEHAVIOR DURING RESET	NOTES
83	XTAL32OUT				None	Output		
84	VSSA_PLL			Ground	None			
85	VDDA_PLL			Power	None			
86	XTALIN				None	Input		4
87	XTALOUT				None	Output		
88	VSSA_ADC			Ground	None			
89	AN3 (LR/Y-)	PJ7			None	Input		
90	AN4 (Wiper)	PJ6			None	Input		
91	AN9	PJ5			None	Input		
92	AN2 (LL/Y+)	PJ4			None	Input		
93	AN8	PJ3			None	Input		
94	AN1 (UR/X-)	PJ2			None	Input		
95	AN6	PJ1			None	Input		
96	AN0 (UL/X+)	PJ0			None	Input		
97	VDDA_ADC			Power	None			
98	VDD			Power	None			
99	PE7	SSPFRM			4 mA	Bidirectional	Pull-up	1
100	PE6	SSPCLK			4 mA	Bidirectional	Pull-down	1
101	PE5	SSPRX			4 mA	Bidirectional	Pull-up	1
102	PE4	SSPTX			4 mA	Bidirectional	Pull-down	1
103	PE3	CANTX	UARTTX0		8 mA	Bidirectional	Pull-up	1
104	PE2	CANRX	UARTRX0		2 mA	Bidirectional	Pull-up	1
105	PE1	UARTTX2			4 mA	Bidirectional	Pull-up	1
106	VSS			Ground	None			
107	PE0	UARTRX2			4 mA	Bidirectional	Pull-up	1
108	PF6	CTCAP2B	CTCMP2B		4 mA	Bidirectional		2
109	PF5	CTCAP2A	CTCMP2A		4 mA	Bidirectional		
110	PF4	CTCAP1B	CACMP1B		4 mA	Bidirectional		2
111	PF3	CTCAP1A	CTCMP1A		4 mA	Bidirectional		
112	VDD			Power	None			
113	PF2	CTCAP0E			4 mA	Bidirectional		2
114	PF1	CTCAP0D			4 mA	Bidirectional		
115	PF0	CTCAP0C			4 mA	Bidirectional		2
116	PG7	CTCAP0B	CTCMP0B		4 mA	Bidirectional		
117	PG6	CTCAP0A	CTCMP0A		4 mA	Bidirectional		2
118	PG5	CTCLK			4 mA	Bidirectional		
119	VSS			Ground	None			
120	PG4	LCDVEEEN			8 mA	Bidirectional		
121	PG3	LCDVDDEN			8 mA	Bidirectional		
122	PG2	LCDDSPLEN			8 mA	Bidirectional		
123	PG1				8 mA	Bidirectional		
124	PG0				8 mA	Bidirectional		

Table 5. LH75400 Numerical Pin List (Cont'd)

PIN NO.	FUNCTION AT RESET	FUNCTION 2	FUNCTION 3	FUNCTION TYPE	OUTPUT DRIVE	BUFFER TYPE	BEHAVIOR DURING RESET	NOTES
125	PH7	LCDDCLK			8 mA	Bidirectional		
126	VDD			Power	None			
127	VSS			Ground	None			
128	PH6	LCDLP			8 mA	Bidirectional		
129	PH5	LCDFP			8 mA	Bidirectional		
130	PH4	LCDEN			8 mA	Bidirectional		
131	PH3	LCDVD11			8 mA	Bidirectional		
132	PH2	LCDVD10			8 mA	Bidirectional		
133	PH1	LCDVD9			8 mA	Bidirectional		
134	VDD			Power	None			
135	PH0	LCDVD8			8 mA	Bidirectional		
136	PI7	LCDVD7			8 mA	Bidirectional		
137	PI6	LCDVD6			8 mA	Bidirectional		
138	PI5	LCDVD5			8 mA	Bidirectional		
139	PI4	LCDVD4			8 mA	Bidirectional		
140	VSS			Ground	None			
141	PI3	LCDVD3			8 mA	Bidirectional		
142	PI2	LCDVD2			8 mA	Bidirectional		
143	PI1	LCDVD1			8 mA	Bidirectional		
144	PI0	LCDVD0			8 mA	Bidirectional		

NOTES:

1. Signal is selectable as pull-up, pull-down, or no pull-up/pull-down via the I/O Configuration peripheral.
2. CMOS Schmitt trigger input.
3. Signals preceded with 'n' are active LOW.
4. Crystal Oscillator Inputs should be driven to 1.8 V ±10% (MAX.)
5. LINREGEN activation requires a 0 Ω pull-up to VDD.

LH75400 Signal Descriptions

Table 6. LH75400 Signal Descriptions

PIN NO.	SIGNAL NAME	TYPE	DESCRIPTION	NOTES
MEMORY INTERFACE (MI)				
1 2 4 5 6 7 9 10 12 13 15 16 18 19 20 21	D[15:0]	Input/Output	Data Input/Output Signals	1
22	nWE	Output	Static Memory Controller Write Enable	2
23	nOE	Output	Static Memory Controller Output Enable	2
24	nWAIT	Input	Static Memory Controller External Wait Control	1, 2
25	nBLE1	Output	Static Memory Controller Byte Lane Strobe	1, 2
27	nBLE0	Output	Static Memory Controller Byte Lane Strobe	1, 2
28	nCS3	Output	Static Memory Controller Chip Select	1, 2
29	nCS2	Output	Static Memory Controller Chip Select	1, 2
30	nCS1	Output	Static Memory Controller Chip Select	1, 2
31	nCS0	Output	Static Memory Controller Chip Select	2
32 33 35 36 37 38 39 40 43 44 45 46 47 49 50 51 52 53 55 56 57 58 60 61	A[23:0]	Output	Address Signals	1
DMA CONTROLLER (DMAC)				
72	DREQ	Input	DMA Request	1
73	DACK	Output	DMA Acknowledge	1

Table 6. LH75400 Signal Descriptions (Cont'd)

PIN NO.	SIGNAL NAME	TYPE	DESCRIPTION	NOTES
LCD CONTROLLER (LCDC)				
120	LCDVEEEN	Output	Analog Supply Enable (AC Bias SIgnal)	1
121	LCDVDDEN	Output	Digital Supply Enable	1
122	LCDDSPLEN	Output	LCD Panel Power Enable	1
125	LCDDCLK	Output	LCD Panel Clock	1
128	LCDLP	Output	Line Synchronization Pulse (STN), Horizontal Synchronization Pulse (TFT)	1
129	LCDFP	Output	Frame Pulse (STN), Vertical Synchronization Pulse (TFT)	1
130	LCDEN	Output	LCD Data Enable	1
131 132 133 135 136 137 138 139 141 142 143 144	LCDVD[11:0]	Output	LCD Panel Data bus	1
SYNCHRONOUS SERIAL PORT (SSP)				
99	SSPFRM	Output	SSP Serial Frame	1
100	SSPCLK	Output	SSP Clock	1
101	SSPRX	Input	SSP RXD	1
102	SSPTX	Output	SSP TXD	1
UART0 (U0)				
103	UARTTX0	Output	UART0 Transmitted Serial Data Output	1
104	UARTRX0	Input	UART0 Received Serial Data Input	1
UART1 (U1)				
74	UARTRX1	Input	UART1 Received Serial Data Input	1
76	UARTTX1	Output	UART1 Transmitted Serial Data Output	1
UART2 (U2)				
105	UARTTX2	Output	UART2 Transmitted Serial Data Output	1
107	UARTRX2	Input	UART2 Received Serial Data Input	1
ANALOG-TO-DIGITAL CONVERTER (ADC)				
89 90 91 92 93 94 95 96	AN3 (LR/Y-) AN4 (Wiper) AN9 AN2 (LL/Y+) AN8 AN1 (UR/X-) AN6 AN0 (UL/X+)	Input	ADC Inputs	1
CONTROLLER AREA NETWORK (CAN)				
103	CANTX	Output	CAN Transmitted Serial Data Output	1
104	CANRX	Input	CAN Received Serial Data Input	1

Table 6. LH75400 Signal Descriptions (Cont'd)

PIN NO.	SIGNAL NAME	TYPE	DESCRIPTION	NOTES
TIMER 0				
117 116 115 114 113	CTCAP0[A:E]	Input	Timer 0 Capture Inputs	1
117 116	CTCMP0[A:B]	Output	Timer 0 Compare Outputs	1
118	CTCLK	Input	Common External Clock	1
TIMER 1				
111 110	CTCAP1[A:B]	Input	Timer 1 Capture Inputs	1
111 110	CTCMP1[A:B]	Output	Timer 1 Compare Outputs	1
118	CTCLK	Input	Common External Clock	1
TIMER 2				
109 108	CTCAP2[A:B]	Input	Timer 2 Capture Inputs	1
109 108	CTCMP2[A:B]	Input	Timer 2 Compare Outputs	1
118	CTCLK	Input	Common External Clock	1
GENERAL PURPOSE INPUT/OUTPUT (GPIO)				
1 2 4 5 6 7 9 10	PA7 PA6 PA5 PA4 PA3 PA2 PA1 PA0	Input/Output	General Purpose I/O Signals - Port A	1
24 25 27 28 29 30	PB5 PB4 PB3 PB2 PB1 PB0	Input/Output	General Purpose I/O Signals - Port B	1
32 33 35 36 37 38 39 40	PC7 PC6 PC5 PC4 PC3 PC2 PC1 PC0	Input/Output	General Purpose I/O Signals - Port C	1
72 73 74 76 77 78 79	PD6 PD5 PD4 PD3 PD2 PD1 PD0	Input/Output	General Purpose I/O Signals - Port D	1

Table 6. LH75400 Signal Descriptions (Cont'd)

PIN NO.	SIGNAL NAME	TYPE	DESCRIPTION	NOTES
89 90 91 92 93 94 95 96	PJ7 PJ6 PJ5 PJ4 PJ3 PJ2 PJ1 PJ0	Input	General Purpose I/O Signals - Port J	1
99 100 101 102 103 104 105 107	PE7 PE6 PE5 PE4 PE3 PE2 PE1 PE0	Input/Output	General Purpose I/O Signals - Port E	1
108 109 110 111 113 114 115	PF6 PF5 PF4 PF3 PF2 PF1 PF0	Input/Output	General Purpose I/O Signals - Port F	1
116 117 118 120 121 122 123 124	PG7 PG6 PG5 PG4 PG3 PG2 PG1 PG0	Input/Output	General Purpose I/O Signals - Port G	1
125 128 129 130 131 132 133 135	PH7 PH6 PH5 PH4 PH3 PH2 PH1 PH0	Input/Output	General Purpose I/O Signals - Port H	1
136 137 138 139 141 142 143 144	PI7 PI6 PI5 PI4 PI3 PI2 PI1 PI0	Input/Output	General Purpose I/O Signals - Port I	1
RESET, CLOCK, AND POWER CONTROLLER (RCPC)				
62	nRESETIN	Input	User Reset Input	2
71	nRESETOUT	Output	System Reset Output	2
72	INT6	Input	External Interrupt Input 6	1
73	INT5	Input	External Interrupt Input 5	1
74	INT4	Input	External Interrupt Input 4	1
76	INT3	Input	External Interrupt Input 3	1
77	INT2	Input	External Interrupt Input 2	1
78	INT1	Input	External Interrupt Input 1	1
79	INT0	Input	External Interrupt Input 0	1

Table 6. LH75400 Signal Descriptions (Cont'd)

PIN NO.	SIGNAL NAME	TYPE	DESCRIPTION	NOTES
81	nPOR	Input	Power-on Reset Input	2
82	XTAL32IN	Input	32.768 kHz Crystal Clock Input	
83	XTAL32OUT	Output	32.768 kHz Crystal Clock Output	
86	XTALIN	Input	Crystal Clock Input	
87	XTALOUT	Output	Crystal Clock Output	
TEST INTERFACE				
63	TEST2	Input	Test Mode Pin 2	
64	TEST1	Input	Test Mode Pin 1	
65	TMS	Input	JTAG Test Mode Select Input	
66	RTCK	Output	Returned JTAG Test Clock Output	
67	TCK	Input	JTAG Test Clock Input	
68	TDI	Input	JTAG Test Serial Data Input	
69	TDO	Output	JTAG Test Data Serial Output	
POWER AND GROUND (GND)				
3 17 34 42 54 98 112 126 134	VDD	Power	I/O Ring VDD	
8 26 41 48 59 106 119 127 140	VSS	Power	I/O Ring VSS	
11 75	VDDC	Power	Core VDD supply (Output if Linear Regulator Enabled, Otherwise Input)	
14 80	VSSC	Power	Core VSS	
70	LINREGEN	Input	Linear Regulator Enable	
84	VSSA_PLL	Power	PLL Analog VSS	
85	VDDA_PLL	Power	PLL Analog VDD Supply	
88	VSSA_ADC	Power	A-to-D converter Analog VSS	
97	VDDA_ADC	Power	A-to-D converter Analog VDD Supply	

NOTES:
1. These pin numbers have multiplexed functions.
2. Signals preceded with 'n' are active LOW.

THE LH75410

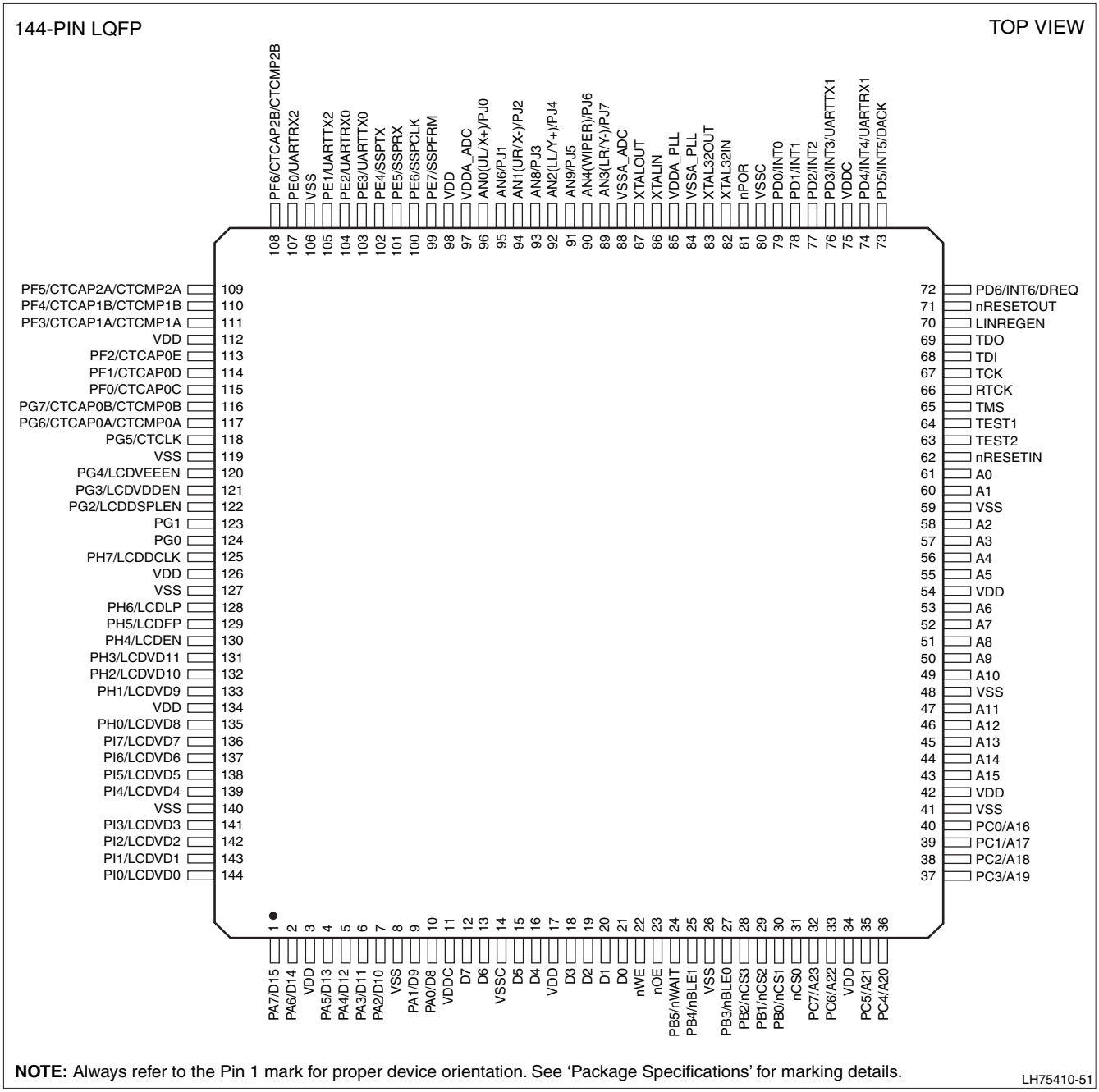


Figure 8. LH75410 Pin Diagram

LH75410 Numerical Pin Listing

Table 7. LH75410 Numerical Pin List

PIN NO.	FUNCTION AT RESET	FUNCTION 2	FUNCTION 3	FUNCTION TYPE	OUTPUT DRIVE	BUFFER TYPE	BEHAVIOR DURING RESET	NOTES
1	PA7	D15		I/O	8 mA	Bidirectional	Pull-up	1
2	PA6	D14		I/O	8 mA	Bidirectional	Pull-up	1
3	VDD			Power	None			
4	PA5	D13		I/O	8 mA	Bidirectional	Pull-up	1
5	PA4	D12		I/O	8 mA	Bidirectional	Pull-up	1
6	PA3	D11		I/O	8 mA	Bidirectional	Pull-up	1
7	PA2	D10		I/O	8 mA	Bidirectional	Pull-up	1
8	VSS			Ground	None			
9	PA1	D9		I/O	8 mA	Bidirectional	Pull-up	1
10	PA0	D8		I/O	8 mA	Bidirectional	Pull-up	1
11	VDDC			Power	None			
12	D7			I/O	8 mA	Bidirectional	Pull-up	
13	D6			I/O	8 mA	Bidirectional	Pull-up	
14	VSSC			Ground	None			
15	D5			I/O	8 mA	Bidirectional	Pull-up	
16	D4			I/O	8 mA	Bidirectional	Pull-up	
17	VDD			Power	None			
18	D3			I/O	8 mA	Bidirectional	Pull-up	
19	D2			I/O	8 mA	Bidirectional	Pull-up	
20	D1			I/O	8 mA	Bidirectional	Pull-up	
21	D0			I/O	8 mA	Bidirectional	Pull-up	
22	nWE				8 mA	Output	HIGH	3
23	nOE				8 mA	Output	HIGH	3
24	PB5	nWAIT			8 mA	Bidirectional	Pull-up	1
25	PB4	nBLE1			8 mA	Bidirectional	Pull-up	1
26	VSS			Ground	None			
27	PB3	nBLE0			8 mA	Bidirectional	Pull-up	1
28	PB2	nCS3			8 mA	Bidirectional	Pull-up	1
29	PB1	nCS2			8 mA	Bidirectional	Pull-up	1
30	PB0	nCS1			8 mA	Bidirectional	Pull-up	1
31	nCS0				8 mA	Output	Pull-up	3
32	PC7	A23			8 mA	Bidirectional	Pull-down	1
33	PC6	A22			8 mA	Bidirectional	Pull-down	1
34	VDD			Power	None			
35	PC5	A21			8 mA	Bidirectional	Pull-down	1
36	PC4	A20			8 mA	Bidirectional	Pull-down	1
37	PC3	A19			8 mA	Bidirectional	Pull-down	1
38	PC2	A18			8 mA	Bidirectional	Pull-down	1
39	PC1	A17			8 mA	Bidirectional	Pull-down	1
40	PC0	A16			8 mA	Bidirectional	Pull-down	1

Table 7. LH75410 Numerical Pin List (Cont'd)

PIN NO.	FUNCTION AT RESET	FUNCTION 2	FUNCTION 3	FUNCTION TYPE	OUTPUT DRIVE	BUFFER TYPE	BEHAVIOR DURING RESET	NOTES
41	VSS			Ground	None			
42	VDD			Power	None			
43	A15				8 mA	Output	LOW	
44	A14				8 mA	Output	LOW	
45	A13				8 mA	Output	LOW	
46	A12				8 mA	Output	LOW	
47	A11				8 mA	Output	LOW	
48	VSS			Ground	None			
49	A10				8 mA	Output	LOW	
50	A9				8 mA	Output	LOW	
51	A8				8 mA	Output	LOW	
52	A7				8 mA	Output	LOW	
53	A6				8 mA	Output	LOW	
54	VDD			Power	None			
55	A5				8 mA	Output	LOW	
56	A4				8 mA	Output	LOW	
57	A3				8 mA	Output	LOW	
58	A2				8 mA	Output	LOW	
59	VSS			Ground	None			
60	A1				8 mA	Output	LOW	
61	A0				8 mA	Output	LOW	
62	nRESETIN				None	Input	Pull-up	2, 3
63	TEST2				None	Input	Pull-up	2
64	TEST1				None	Input	Pull-up	2
65	TMS				None	Input	Pull-up	2
66	RTCK				4 mA	Output		
67	TCK				None	Input		
68	TDI				None	Input	Pull-up	2
69	TDO				4 mA	Output		
70	LINREGEN				None	Input		5
71	nRESETOUT				8 mA	Output		3
72	PD6	INT6	DREQ		6 mA	Bidirectional	Pull-down	1
73	PD5	INT5	DACK		6 mA	Bidirectional		1, 2
74	PD4	INT4	UARTRX1		8 mA	Bidirectional	Pull-up	1
75	VDDC			Power	None			
76	PD3	INT3	UARTTX1		8 mA	Bidirectional	Pull-up	1
77	PD2	INT2			2 mA	Bidirectional	Pull-up	1
78	PD1	INT1			6 mA	Bidirectional		1, 2
79	PD0	INT0			2 mA	Bidirectional		1
80	VSSC			Ground	None			
81	nPOR				None	Input	Pull-up	2, 3
82	XTAL32IN				None	Output		4

Table 7. LH75410 Numerical Pin List (Cont'd)

PIN NO.	FUNCTION AT RESET	FUNCTION 2	FUNCTION 3	FUNCTION TYPE	OUTPUT DRIVE	BUFFER TYPE	BEHAVIOR DURING RESET	NOTES
83	XTAL32OUT				None	Output		
84	VSSA_PLL			Ground	None			
85	VDDA_PLL			Power	None			
86	XTALIN				None	Input		4
87	XTALOUT				None	Output		
88	VSSA_ADC			Ground	None			
89	AN3 (LR/Y-)	PJ7			None	Input		
90	AN4 (Wiper)	PJ6			None	Input		
91	AN9	PJ5			None	Input		
92	AN2 (LL/Y+)	PJ4			None	Input		
93	AN8	PJ3			None	Input		
94	AN1 (UR/X-)	PJ2			None	Input		
95	AN6	PJ1			None	Input		
96	AN0 (UL/X+)	PJ0			None	Input		
97	VDDA_ADC			Power	None			
98	VDD			Power	None			
99	PE7	SSPFRM			4 mA	Bidirectional	Pull-up	1
100	PE6	SSPCLK			4 mA	Bidirectional	Pull-down	1
101	PE5	SSPRX			4 mA	Bidirectional	Pull-up	1
102	PE4	SSPTX			4 mA	Bidirectional	Pull-down	1
103	PE3	UARTTX0			8 mA	Bidirectional	Pull-up	1
104	PE2	UARTRX0			2 mA	Bidirectional	Pull-up	1
105	PE1	UARTTX2			4 mA	Bidirectional	Pull-up	1
106	VSS			Ground	None			
107	PE0	UARTRX2			4 mA	Bidirectional	Pull-up	1
108	PF6	CTCAP2B	CTCMP2B		4 mA	Bidirectional		2
109	PF5	CTCAP2A	CTCMP2A		4 mA	Bidirectional		
110	PF4	CTCAP1B	CACMP1B		4 mA	Bidirectional		2
111	PF3	CTCAP1A	CTCMP1A		4 mA	Bidirectional		
112	VDD			Power	None			
113	PF2	CTCAP0E			4 mA	Bidirectional		2
114	PF1	CTCAP0D			4 mA	Bidirectional		
115	PF0	CTCAP0C			4 mA	Bidirectional		2
116	PG7	CTCAP0B	CTCMP0B		4 mA	Bidirectional		
117	PG6	CTCAP0A	CTCMP0A		4 mA	Bidirectional		2
118	PG5	CTCLK			4 mA	Bidirectional		
119	VSS			Ground	None			
120	PG4	LCDVEEEN			8 mA	Bidirectional		
121	PG3	LCDVDDEN			8 mA	Bidirectional		
122	PG2	LCDDSPLEN			8 mA	Bidirectional		
123	PG1				8 mA	Bidirectional		
124	PG0				8 mA	Bidirectional		

Table 7. LH75410 Numerical Pin List (Cont'd)

PIN NO.	FUNCTION AT RESET	FUNCTION 2	FUNCTION 3	FUNCTION TYPE	OUTPUT DRIVE	BUFFER TYPE	BEHAVIOR DURING RESET	NOTES
125	PH7	LCDDCLK			8 mA	Bidirectional		
126	VDD			Power	None			
127	VSS			Ground	None			
128	PH6	LCDLP			8 mA	Bidirectional		
129	PH5	LCDFP			8 mA	Bidirectional		
130	PH4	LCDEN			8 mA	Bidirectional		
131	PH3	LCDVD11			8 mA	Bidirectional		
132	PH2	LCDVD10			8 mA	Bidirectional		
133	PH1	LCDVD9			8 mA	Bidirectional		
134	VDD			Power	None			
135	PH0	LCDVD8			8 mA	Bidirectional		
136	PI7	LCDVD7			8 mA	Bidirectional		
137	PI6	LCDVD6			8 mA	Bidirectional		
138	PI5	LCDVD5			8 mA	Bidirectional		
139	PI4	LCDVD4			8 mA	Bidirectional		
140	VSS			Ground	None			
141	PI3	LCDVD3			8 mA	Bidirectional		
142	PI2	LCDVD2			8 mA	Bidirectional		
143	PI1	LCDVD1			8 mA	Bidirectional		
144	PI0	LCDVD0			8 mA	Bidirectional		

NOTES:

1. Signal is selectable as pull-up, pull-down, or no pull-up/pull-down via the I/O Configuration peripheral.
2. CMOS Schmitt trigger input.
3. Signals preceded with 'n' are active LOW.
4. Crystal Oscillator Inputs should be driven to 1.8 V ±10% (MAX.)
5. LINREGEN activation requires a 0 Ω pull-up to VDD.

LH75410 Signal Descriptions

Table 8. LH75410 Signal Descriptions

PIN NO.	SIGNAL NAME	TYPE	DESCRIPTION	NOTES
MEMORY INTERFACE (MI)				
1 2 4 5 6 7 9 10 12 13 15 16 18 19 20 21	D[15:0]	Input/Output	Data Input/Output Signals	1
22	nWE	Output	Static Memory Controller Write Enable	2
23	nOE	Output	Static Memory Controller Output Enable	2
24	nWAIT	Input	Static Memory Controller External Wait Control	1, 2
25	nBLE1	Output	Static Memory Controller Byte Lane Strobe	1, 2
27	nBLE0	Output	Static Memory Controller Byte Lane Strobe	1, 2
28	nCS3	Output	Static Memory Controller Chip Select	1, 2
29	nCS2	Output	Static Memory Controller Chip Select	1, 2
30	nCS1	Output	Static Memory Controller Chip Select	1, 2
31	nCS0	Output	Static Memory Controller Chip Select	2
32 33 35 36 37 38 39 40 43 44 45 46 47 49 50 51 52 53 55 56 57 58 60 61	A[23:0]	Output	Address Signals	1
DMA CONTROLLER (DMAC)				
72	DREQ	Input	DMA Request	1
73	DACK	Output	DMA Acknowledge	1

Table 8. LH75410 Signal Descriptions (Cont'd)

PIN NO.	SIGNAL NAME	TYPE	DESCRIPTION	NOTES
LCD CONTROLLER (LCDC)				
120	LCDVEEEN	Output	Analog Supply Enable (AC Bias SIgnal)	1
121	LCDVDDEN	Output	Digital Supply Enable	1
122	LCDDSPLEN	Output	LCD Panel Power Enable	1
125	LCDDCLK	Output	LCD Panel Clock	1
128	LCDLP	Output	Line Synchronization Pulse (STN), Horizontal Synchronization Pulse (TFT)	1
129	LCDFP	Output	Frame Pulse (STN), Vertical Synchronization Pulse (TFT)	1
130	LCDEN	Output	LCD Data Enable	1
131 132 133 135 136 137 138 139 141 142 143 144	LCDVD[11:0]	Output	LCD Panel Data bus	1
SYNCHRONOUS SERIAL PORT (SSP)				
99	SSPFRM	Output	SSP Serial Frame	1
100	SSPCLK	Output	SSP Clock	1
101	SSPRX	Input	SSP RXD	1
102	SSPTX	Output	SSP TXD	1
UART0 (U0)				
103	UARTTX0	Output	UART0 Transmitted Serial Data Output	1
104	UARTRX0	Input	UART0 Received Serial Data Input	1
UART1 (U1)				
74	UARTRX1	Input	UART1 Received Serial Data Input	1
76	UARTTX1	Output	UART1 Transmitted Serial Data Output	1
UART2 (U2)				
105	UARTTX2	Output	UART2 Transmitted Serial Data Output	1
107	UARTRX2	Input	UART2 Received Serial Data Input	1
ANALOG-TO-DIGITAL CONVERTER (ADC)				
89 90 91 92 93 94 95 96	AN3 (LR/Y-) AN4 (Wiper) AN9 AN2 (LL/Y+) AN8 AN1 (UR/X-) AN6 AN0 (UL/X+)	Input	ADC Inputs	1
TIMER 0				
117 116 115 114 113	CTCAP0[A:E]	Input	Timer 0 Capture Inputs	1
117 116	CTCMP0[A:B]	Output	Timer 0 Compare Outputs	1
118	CTCLK	Input	Common External Clock	1

Table 8. LH75410 Signal Descriptions (Cont'd)

PIN NO.	SIGNAL NAME	TYPE	DESCRIPTION	NOTES
TIMER 1				
111 110	CTCAP1[A:B]	Input	Timer 1 Capture Inputs	1
111 110	CTCMP1[A:B]	Output	Timer 1 Compare Outputs	1
118	CTCLK	Input	Common External Clock	1
TIMER 2				
109 108	CTCAP2[A:B]	Input	Timer 2 Capture Inputs	1
109 108	CTCMP2[A:B]	Input	Timer 2 Compare Outputs	1
118	CTCLK	Input	Common External Clock	1
GENERAL PURPOSE INPUT/OUTPUT (GPIO)				
1 2 4 5 6 7 9 10	PA7 PA6 PA5 PA4 PA3 PA2 PA1 PA0	Input/Output	General Purpose I/O Signals - Port A	1
24 25 27 28 29 30	PB5 PB4 PB3 PB2 PB1 PB0	Input/Output	General Purpose I/O Signals - Port B	1
32 33 35 36 37 38 39 40	PC7 PC6 PC5 PC4 PC3 PC2 PC1 PC0	Input/Output	General Purpose I/O Signals - Port C	1
72 73 74 76 77 78 79	PD6 PD5 PD4 PD3 PD2 PD1 PD0	Input/Output	General Purpose I/O Signals - Port D	1
89 90 91 92 93 94 95 96	PJ7 PJ6 PJ5 PJ4 PJ3 PJ2 PJ1 PJ0	Input	General Purpose I/O Signals - Port J	1
99 100 101 102 103 104 105 107	PE7 PE6 PE5 PE4 PE3 PE2 PE1 PE0	Input/Output	General Purpose I/O Signals - Port E	1

Table 8. LH75410 Signal Descriptions (Cont'd)

PIN NO.	SIGNAL NAME	TYPE	DESCRIPTION	NOTES
108 109 110 111 113 114 115	PF6 PF5 PF4 PF3 PF2 PF1 PF0	Input/Output	General Purpose I/O Signals - Port F	1
116 117 118 120 121 122 123 124	PG7 PG6 PG5 PG4 PG3 PG2 PG1 PG0	Input/Output	General Purpose I/O Signals - Port G	1
125 128 129 130 131 132 133 135	PH7 PH6 PH5 PH4 PH3 PH2 PH1 PH0	Input/Output	General Purpose I/O Signals - Port H	1
136 137 138 139 141 142 143 144	PI7 PI6 PI5 PI4 PI3 PI2 PI1 PI0	Input/Output	General Purpose I/O Signals - Port I	1
RESET, CLOCK, AND POWER CONTROLLER (RCPC)				
62	nRESETIN	Input	User Reset Input	2
71	nRESETOUT	Output	System Reset Output	2
72	INT6	Input	External Interrupt Input 6	1
73	INT5	Input	External Interrupt Input 5	1
74	INT4	Input	External Interrupt Input 4	1
76	INT3	Input	External Interrupt Input 3	1
77	INT2	Input	External Interrupt Input 2	1
78	INT1	Input	External Interrupt Input 1	1
79	INT0	Input	External Interrupt Input 0	1
81	nPOR	Input	Power-on Reset Input	2
82	XTAL32IN	Input	32.768 kHz Crystal Clock Input	
83	XTAL32OUT	Output	32.768 kHz Crystal Clock Output	
86	XTALIN	Input	Crystal Clock Input	
87	XTALOUT	Output	Crystal Clock Output	

Table 8. LH75410 Signal Descriptions (Cont'd)

PIN NO.	SIGNAL NAME	TYPE	DESCRIPTION	NOTES
TEST INTERFACE				
63	TEST2	Input	Test Mode Pin 2	
64	TEST1	Input	Test Mode Pin 1	
65	TMS	Input	JTAG Test Mode Select Input	
66	RTCK	Output	Returned JTAG Test Clock Output	
67	TCK	Input	JTAG Test Clock Input	
68	TDI	Input	JTAG Test Serial Data Input	
69	TDO	Output	JTAG Test Data Serial Output	
POWER AND GROUND (GND)				
3 17 34 42 54 98 112 126 134	VDD	Power	I/O Ring VDD	
8 26 41 48 59 106 119 127 140	VSS	Power	I/O Ring VSS	
11 75	VDDC	Power	Core VDD supply (Output if Linear Regulator Enabled, Otherwise Input)	
14 80	VSSC	Power	Core VSS	
70	LINREGEN	Input	Linear Regulator Enable	
84	VSSA_PLL	Power	PLL Analog VSS	
85	VDDA_PLL	Power	PLL Analog VDD Supply	
88	VSSA_ADC	Power	A-to-D converter Analog VSS	
97	VDDA_ADC	Power	A-to-D converter Analog VDD Supply	

NOTES:
1. These pins have multiplexed functions.
2. Signals preceded with 'n' are active LOW.

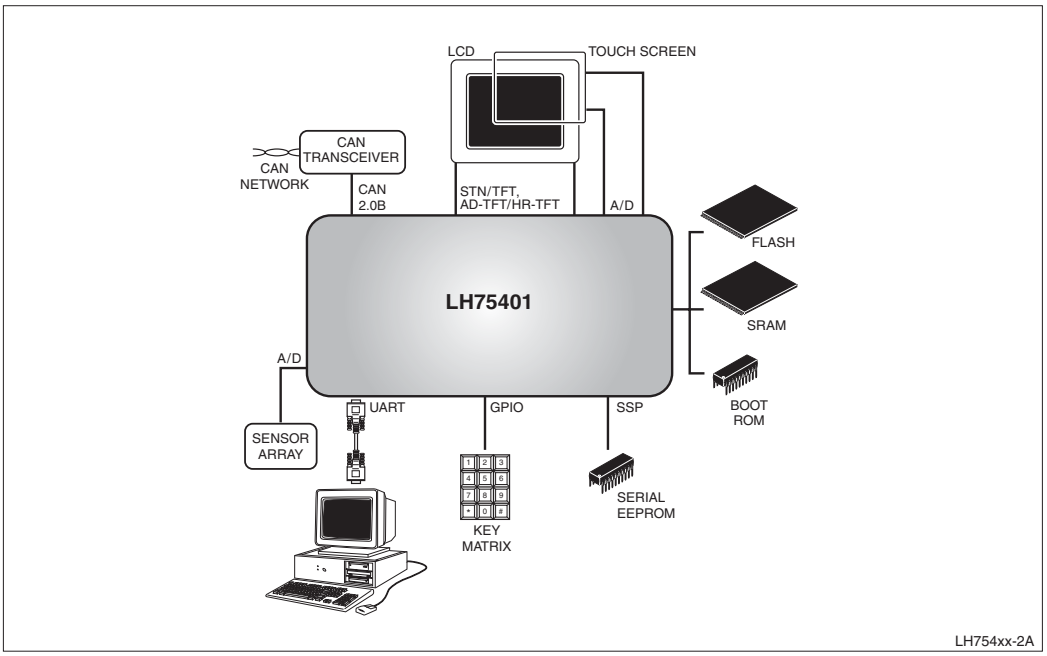


Figure 9. LH75401 System Application Example

FUNCTIONAL OVERVIEW

ARM7TDMI-S Processor

The LH75400/01/10/11 microcontrollers feature the ARM7TDMI-S core with an Advanced High-Performance Bus (AHB) 2.0 interface. The ARM7TDMI-S is a 16/32-bit embedded RISC processor and a member of the ARM7 Thumb family of processors. For more information, visit the ARM Web site at www.arm.com.

Bus Architecture

The LH75400/01/10/11 microcontrollers use the ARM Advanced Microcontroller Bus Architecture (AMBA) 2.0 internal bus protocol. Three AHB masters control access to external memory and on-chip peripherals:

- The ARM processor fetches instructions and transfers data
- The Direct Memory Access Controller (DMAC) transfers from memory to memory, from peripheral to memory, and from memory to peripheral
- The LCDC refreshes an LCD panel with data from the external memory or from internal memory if the frame buffer is 16KB or less.

The ARM7TDMI-S processor is the default bus master. An Advanced Peripheral Bus (APB) bridge is provided to access to the various APB peripherals. Generally, APB peripherals are serviced by the ARM core. However, if they are DMA-enabled, they are also serviced by the DMAC to increase system performance while the ARM core runs from local internal memory.

Power Supplies

Five-Volt-tolerant 3.3 V I/Os are employed. The LH75400/01/10/11 microcontrollers require a single 3.3 V supply. The core logic requires 1.8 V, supplied by an on-chip linear regulator. Core logic power may also be supplied externally to achieve higher system speeds. See the Electrical Specifications.

Clock Sources

The LH75400/01/10/11 microcontrollers may use two crystal oscillators, or an externally supplied clock. There are two clock trees:

- One clock tree drives an internal Phase Lock Loop (PLL) and the three UARTs. It supports a crystal oscillator frequency range from 14 MHz to 20 MHz.
- The other is a 32.768 kHz oscillator that generates a 1 Hz clock for the RTC. (Use of the 32.768 kHz crystal for the Real Time Clock is optional. If not using the crystal, tie XTAL32IN to VSS and allow XTAL32OUT to float.)

The 14-to-20 MHz crystal oscillator drives the UART clocks, so an oscillator frequency of 14.7456 MHz is recommended to achieve modem baud rates.

The PLL may be bypassed and an external clock supplied at XTALIN; the SoC will operate to DC with the PLL disabled. When doing so, allow XTALOUT to float. The input clock with the PLL bypassed will be twice the desired system operating frequency, and care must be taken not to exceed the maximum input clock voltage. Maximum values for system speeds and input voltages are given in the Electrical Specifications.

Reset Generation

EXTERNAL RESETS

Two external signals generate resets to the ARM7TDMI-S core:

- nPOR sets all internal registers to their default state when asserted. It is used as a Power-On Reset.
- nRESETIN sets all internal registers, except the JTAG circuitry, to their default state when asserted.

When nPOR is asserted, nRESETIN defines the microcontroller Test Mode. When nPOR is released, nRESETIN behaves during Reset as described previously.

INTERNAL RESETS

There are two types of Internal Resets generated:

- System Reset
- RTC Reset.

System and RTC Resets are asserted by:

- An External Reset (a logic LOW signal on the external nRESETIN or nPOR input pin)
- A signal from the internal Watchdog Timer
- A Soft Reset.

The reset latency depends on the PLL lock state.

AHB Master Priority and Arbitration

The LH75400/01/10/11 microcontrollers have three AHB masters:

- ARM processor
- DMAC
- LCD Controller.

Each AHB master has a priority level that is permanent and cannot change.

Table 9. Bus Master Priority

PRIORITY	BUS MASTER PRIORITY
1 (Highest)	Color LCDC (LH75401 and LH75411) LCDC (LH75400 and LH75410)
2	DMAC
3 (Lowest)	ARM7TDMI-S Core (Default)

Memory Interface Architecture

The LH75400/01/10/11 microcontrollers provide the following data-path management resources on chip:

- AHB and APB data buses
- 16KB of zero-wait-state TCM SRAM accessible via processor
- 16KB of internal SRAM accessible via processor, DMAC, and LCDC
- A Static Memory Controller (SMC) that controls access to external memory
- A 4-stream general-purpose DMAC.

All external and internal system resources are memory-mapped. This memory map partition has three views, based on the setting of the REMAP bits in the Reset, Clock, and Power Controller (RCPC).

The second partitioning of memory space is the dividing of the segments into sections. The external memory segment is divided into eight 64MB sections, of which the first four are used, each having a chip select associated with it. Access to any of the last four sections does not result in an external bus access and does not cause a memory abort. The peripheral register segment is divided into 4KB peripheral sections, 21 of which are assigned to peripherals.

Table 10. Memory Mapping

ADDRESS	REMAP = 00 (DEFAULT)	REMAP = 01	REMAP = 10
0x00000000	External Memory	Internal SRAM	TCM SRAM
0x20000000	Reserved	Reserved	Reserved
0x40000000	External Memory	External Memory	External Memory
0x60000000	Internal SRAM	Internal SRAM	Internal SRAM
0x80000000	TCM SRAM	TCM SRAM	TCM SRAM
0xA0000000	Reserved	Reserved	Reserved
0xC0000000	Reserved	Reserved	Reserved
0xE0000000 - 0xFFFBFFFF	Reserved	Reserved	Reserved

Table 11. APB Peripheral Register Mapping

ADDRESS RANGE	DEVICE
0xFFFC0000 - 0xFFFC0FFF	UART0 (16550)
0xFFFC1000 - 0xFFFC1FFF	UART1 (16550)
0xFFFC2000 - 0xFFFC2FFF	UART2 (82510)
0xFFFC3000 - 0xFFFC3FFF	Analog-to-Digital Converter
0xFFFC4000 - 0xFFFC4FFF	Timer Module
0xFFFC5000 - 0xFFFC5FFF	CAN (LH75401/LH75400) Reserved (LH75411/LH75410)
0xFFFC6000 - 0xFFFC6FFF	Synchronous Serial Port
0xFFFC7000 - 0xFFFDAFFF	Reserved
0xFFFDB000 - 0xFFFDBFFF	GPIO4
0xFFFDC000 - 0xFFFDCFFF	GPIO3
0xFFFDD000 - 0xFFFDDFFF	GPIO2
0xFFFDE000 - 0xFFFDEFFF	GPIO1
0xFFFDF000 - 0xFFFDFFFF	GPIO0
0xFFFE0000 - 0xFFFE0FFF	Real Time Clock
0xFFFE1000 - 0xFFFE1FFF	DMAC
0xFFFE2000 - 0xFFFE2FFF	Reset Clock and Power Controller
0xFFFE3000 - 0xFFFE3FFF	Watchdog Timer
0xFFFE4000 - 0xFFFE4FFF	Advanced LCD Interface
0xFFFE5000 - 0xFFFE5FFF	I/O Configuration Peripheral
0xFFFE6000 - 0xFFFEFFFF	Reserved

Static Random Access Memory Controller

The LH75400/01/10/11 microcontrollers have 32KB of Static Random Access Memory (SRAM) organized into two 16KB blocks:

- 16KB of TCM 0 Wait State SRAM is available to the processor as an ARM7TDMI-S bus slave.
- 16KB of internal SRAM is available as an AHB slave and accessible via processor, DMAC, and LCDC.

Each memory segment is 512MB, though the TCM and internal SRAMs are 16KB each in size. Any access beyond the first 16KB is mapped to the lower 16KB, but does not cause a data or prefetch abort.

Static Memory Controller (SMC)

The Static Memory Controller (SMC) is an AMBA AHB slave peripheral that provides the interface between the LH75400/01/10/11 microcontrollers and external memory devices.

SMC FEATURES

- Provides four banks of external memory, each with a maximum size of 16MB.
- Supports memory-mapped devices, including Random Access Memory (RAM), Read Only Memory (ROM), Flash, and burst ROM
- Supports external bus and external device widths of 8 and 16 bits
- Supports Asynchronous Burst Mode read access for Burst Mode ROM devices, with up to 32 independent wait states for read and write accesses
- Supports indefinite extended wait states via an external hardware pin (nWAIT)
- Supports varied bus turnaround cycles (1 to 16) between a read and write operation

Direct Memory Access Controller (DMAC)

One central DMAC services all peripheral DMA requirements for the DMA-capable peripherals listed in Table 12.

The DMA is controlled by the system clock. It has an APB slave port for programming of its registers and an AHB port for data transfers.

Table 12. DMAC Stream Assignments

DMA REQUEST SOURCE	DMA STREAM
UART1RX (highest priority)	Stream0
UART1TX	Stream1
UART0RX/External Request (DREQ)	Stream2
UART0TX (lowest priority)	Stream3

DMAC FEATURES

- Four data streams that can be used to service:
  - Four peripheral data streams (peripheral-to-memory or memory-to-peripheral)
  - Three peripheral data streams and one memory-to-memory data stream.
- Three transfer modes:
  - Memory to Memory (selectable on Stream3)
  - Peripheral to Memory (all streams)
  - Memory to Peripheral (all streams).
- Built-in data stream arbiter
- Seven programmable registers for each stream
- Ability for each stream to indicate a transfer error via an interrupt
- 16-word First-In, First Out (FIFO) array, with pack and unpack logic to handle all input/output combinations of byte, half-word, and word transfers
- APB slave port allows the ARM core to program DMAC registers
- AHB port for data transfers.

Color LCD Controller (CLCDC)

The CLCDC is an AMBA master-slave module that connects to the AHB. It translates pixel-coded data into the required formats and timings to drive single/dual monochrome and color LCD panels. Packets of pixel-coded data are fed, via the AHB interface, to two independently programmable, 32-bit-wide DMA FIFOs. Each FIFO is 16 words deep by 32 bits wide.

The CLCDC generates a single combined interrupt to the Vectored Interrupt Controller (VIC) when an interrupt condition becomes true for upper/lower panel DMA FIFO underflow, base address update signification, vertical compare, or bus error.

NOTE: LH75401 and LH75411 microcontrollers support full-colo operation. LH75400 and LH75410 microcontrollers are monochrome only.

CLCDC FEATURES

- STN, Color STN, TFT, HR-TFT, and AD-TFT
  - Fully Programmable Timing Controls
  - Advanced LCD Interface for displays with a low level of integration, such as HR-TFT and AD-TFT
- Programmable Resolution
  - Up to VGA (640 × 480 DPI), 12-bit Direct Mode Color
  - Up to SVGA (800 × 600 DPI), 8-bit Direct/Paletized Color
  - Up to XGA (1,024 × 768 DPI), 4-bit Direct Color/ Grayscale
  - Direct or Paletized Colors
- Single and Dual Panels
- Supports Sharp and non-Sharp Panels
- CLCDC Outputs Available as General Purpose Inputs/Outputs (GPIOs) if LCDC is Not Needed
- Additional Features
  - Fully programmable horizontal and vertical timing for different display panels
  - 256-entry, 16-bit palette RAM physically arranged as a 128 × 32-bit RAM
  - AC bias signal for STN panels and a data-enable signal for TFT panels.
- Programmable Panel-related Parameters
  - STN mono/color or TFT display
  - Bits-per-pixel
  - STN 4- or 8-bit Interface Mode
  - STN Dual or Single Panel Mode
  - AC panel bias
  - Panel clock frequency
  - Number of panel clocks per line
  - Signal polarity, active HIGH or LOW
  - Little Endian data format
  - Interrupt-generation event.

ADVANCED LCD INTERFACE

The Advanced LCD Interface (ALI) allows for direct connection to ultra-thin panels that do not include a timing ASIC. It converts TFT signals from the Color LCD controller to provide the proper signals, timing and levels for direct connection to a panel's Row and Column drivers for AD-TFT, HR-TFT, or any technology of panel that allows for a connection of this type. The ALI also provides a bypass mode that allows interfacing to the built-in timing ASIC in standard TFT and STN panels.

NOTES:
1. The Advanced LCD Interface pertains to the LH75401 and LH75411 microcontrollers.
2. VGA and XGA modes require 66 MHz core speed.

Universal Asynchronous Receiver Transmitters (UARTs)

The LH75400/01/10/11 microcontrollers incorporate three UARTs, designated UART0, UART1, and UART2.

UART 0 AND 1 FEATURES

- Similar functionality to the industry-standard 16C550
- Supported baud rates up to 921,600 baud (given an external crystal frequency of 14.756 MHz)
- Supported character formats:
  - Data bits per character: 5, 6, 7, or 8
  - Parity generation and detection: Even, odd, stick, or none
  - Stop bit generation: 1 or 2
- Full-duplex operation
- Separate transmit and receive FIFOs, with:
  - Programmable depth (1 to 16)
  - Programmable-service 'trigger levels' (1/8, 1/4, 1/2, 3/4, and 7/8)
  - Overrun protection.
- Programmable baud-rate generator that:
  - Enables the UART input clock to be divided by 16 to 65,535 × 16
  - Generates an internal clock common to both transmit and receive portions of the UART.
- DMA support
- Support for generating and detecting breaks during UART transactions
- Loopback testing.

UART 2 FEATURES

- Similar functionality to the industry-standard 82510
- Supported baud rates up to 3,225,600 baud (given a system clock of 51.6096 MHz)
- 5, 6, 7, 8, or 9 data bits per character
- Even, odd, HIGH, LOW, software, or no parity-bit generation and detection
- 3/4, 1, 1-1/4, 1-1/2, 1-3/4, or 2 stop-bit generation
- µLAN address flag
- Full-duplex operation
- Separate transmit and receive FIFOs, with programmable depth (1 or 4). Each FIFO has overrun protection and:
  - Programmable receive trigger levels: 1/4, 1/2, 3/4, or full
  - Programmable transmit trigger levels: empty, 1/4, 1/2, 3/4.
- Two 16-bit baud-rate generators.
- One interrupt that can be triggered by transmit and receive FIFO thresholds, receive errors, control character or address marker reception, or timer timeout
- Generation and detection of breaks during UART transactions
- Support for local loopback, remote loopback, and auto-echo modes
- µLAN Address Mode.

Timers

The LH75400/01/10/11 microcontrollers have three 16-bit timers. The timers are clocked by the system clock, but have an internal scaled-down system clock that is used for the Pulse Width Modulator (PWM) and compare functions.

All counters are incremented by an internal prescaled counter clock or external clock and can generate an overflow interrupt. All three timers have separate internal prescaled counter clocks, with either a common external clock or a prescaled version of the system clock.

- Timer 0 has five Capture Registers and two Compare Registers.
- Timer 1 and Timer 2 have two Capture and two Compare Registers each.

The Capture Registers have edge-selectable inputs and can generate an interrupt. The Compare Registers can force the compare output pin either HIGH or LOW upon a match.

The timers support a PWM Mode that uses the two Timer Compare Registers associated with a timer to create a PWM. Each timer can generate a separate interrupt. The interrupt becomes active if any enabled compare, capture, or overflow interrupt condition occurs. The interrupt remains active until all compare, capture, and overflow interrupts are cleared.

Real Time Clock (RTC)

The RTC is an AMBA slave module that connects to the APB. The RTC provides basic alarm functions or acts as a long-time base counter by generating an interrupt signal after counting for a programmed number of cycles of an RTC input. Counting in 1-second intervals is achieved using a 1 Hz clock input to the RTC.

RTC FEATURES

- 32-bit up-counter with programmable load
- Programmable 32-bit match Compare Register
- Software-maskable interrupt that is set when the Counter and Compare Registers have identical values.

Controller Area Network (CAN)

The CAN 2.0B Controller is an AMBA-compliant peripheral that connects as a slave to the APB. The CAN Controller is located between the processor core and a CAN Transceiver, and is accessed through the AMBA port.

CAN communications are performed serially, at a maximum frequency of 1MB/s, using the TX (transmit) and RX (receive) lines. The TX and RX signals for data transmission and reception provide the communications interface between the CAN Controller and the CAN bus. All peripherals share the TX and RX lines, and always see the common incoming and outgoing data.

Bus arbitration follows the CAN 2.0A and CAN 2.0B specifications. The bus is always controlled by the node with the highest priority (lowest ID). Only after the bus has been released can the next highest priority node control it. Transmit and receive errors are handled according to the CAN protocol.

Bus timing is critical to the CAN protocol. Therefore, the CAN Controller has two programmable Bus Timing Registers that define timing parameters.

NOTE: The CAN Controller pertains to the LH75401 and LH75400 microcontrollers.

CAN 2.0B FEATURES

- Full compliance with 2.0A and 2.0B Bosch specifications
- Supports 11-bit and 29-bit identifiers
- Supports bit rates up to 1Mbit/s
- 64-byte receive FIFO
- Software-driven bit-rate detection for hot plug-in support
- Single-shot transmission option
- Acceptance filtering
- Listen Only Mode
- Reception of 'own' messages
- Error interrupt generated for each CAN bus error
- Arbitration-lost interrupt with record of bit position
- Read/write error counters
- Last error register
- Programmable error-limit warning.

Analog-to-Digital Converter (ADC)/ Brownout Detector

The ADC is an AMBA-compliant peripheral that connects as a slave to the APB. The ADC block consists of an 8-channel, 10-bit Analog-to-Digital Converter with integrated Touch Screen Controller. The complete Touch Screen interface is achieved by combining the front-end biasing, control circuitry with analog-to-digital conversion, reference generation, and digital control.

The ADC also has a programmable measurement clock derived from the system clock. The clock drives the measurement sequencer and the successive-approximation circuitry.

The ADC includes a Brownout Detector. The Brownout Detector is an asynchronous comparator that compares a divided version of the 3.3 V supply and a bandgap-derived reference voltage. If the supply dips below a Trip point, the Brownout Detector sets a status register bit. The status bit is wired to the VIC and can interrupt the processor core. This allows the Host Controller to warn users of an impending shutdown and may provide the ADC with sufficient time to save its state.

ADC/BROWNOUT DETECTOR FEATURES

- 10-bit fully differential Successive Approximation Register (SAR) with integrated sample/hold
- 8-channel multiplexer for routing user-selected inputs to the ADC in Single Ended and Differential Modes
- 16-entry × 16-bit-wide FIFO that holds the 10-bit ADC output and a 4-bit tag number
- Front bias-and-control network for Touch Screen interface and support functions compatible with industry-standard 4- and 5-wire touch-sensitive panels
- Touch-pressure sensing circuits
- Pen-down sensing circuit and interrupt generator
- Voltage-reference generator that is independently controlled
- Conversion automation function to minimize controller interrupt overhead
- Brownout Detector.

Synchronous Serial Port (SSP)

The SSP is a master-only interface for synchronous serial communication with slave peripheral devices that have a Motorola SPI, National Semiconductor Microwire, or Texas Instruments DSP-compatible Synchronous Serial Interface (SSI).

The SSP performs serial-to-parallel conversion on data received from a peripheral device. The transmit and receive paths are buffered with internal FIFO memories. These memories store eight 16-bit values independently in both transmit and receive modes. During transmission:

- Data writes to the transmit FIFO via the APB interface.
- The transmit data is queued for parallel-to-serial conversion onto the transmit interface.
- The transmit logic formats the data into the appropriate frame type:
  - Motorola SPI
  - National Semiconductor Microwire
  - Texas Instruments DSP-compatible SSI.

SSP FEATURES

- SSI in Master Only Mode. The SSP performs serial communications as a master device in one of three modes:
  - Motorola SPI
  - Texas Instruments DSP-compatible synchronous serial interface
  - National Semiconductor Microwire.
- Two 16-bit-wide, 8-entry-deep FIFOs, one for data transmission and one for data reception.
- Supports interrupt-driven data transfers that are greater than the FIFO watermark.
- Programmable clock bit rate.
- Programmable data frame size, from 4 to 16 bits long, depending on the size of data programmed. Each frame transmits starting with the most-significant bit.
- Four interrupts, each of which can be individually enabled or disabled using the SSP Control Register bits. A combined interrupt is also generated as an OR function of the individual interrupt requests.
- Loopback Test Mode.

Table 13. SSP Modes

MODE	DESCRIPTION	DATA TRANSFERS
Motorola SPI	For communications with Motorola SPI-compatible devices. Clock polarity and phase are programmable.	Full-duplex, 4-wire synchronous
SSI	For communications with Texas Instruments DSP-compatible Serial Synchronous Interface devices.	Full-duplex, 4-wire synchronous
National Semiconductor Microwire	For communications with National Semiconductor Microwire-compatible devices.	Half-duplex synchronous, using 8-bit control messages

Watchdog Timer (WDT)

The WDT consists of a 32-bit down-counter that allows a selectable time-out interval to detect malfunctions. The timer must be reset by software periodically. Otherwise, a time-out occurs, interrupting the system. If the interrupt is not serviced within the timeout period, the WDT triggers the RCPC to generate a System Reset. If the WDT times out, it sets a bit in the RCPC Reset Status Register.

The WDT supports 16 selectable time intervals, for a time-out of 216 through 231 system clock cycles. All Control and Status Registers for the Watchdog Timer are accessed through the APB.

WDT FEATURES

- Counter generates an interrupt at a set interval and the count reloads from the pre-set value after reaching zero.
- Default timeout period is set to the minimum timeout of 216 system clock cycles.
- WDT is driven by the APB.
- Built-in protection mechanism guards against interrupt-service failure.
- WDT can be programmed to trigger a System Reset on a timeout.
- WDT can be programmed to trigger an interrupt on the first timeout; then, if the service routine fails to clear the interrupt, the next WDT timeout triggers a System Reset.

Vectored Interrupt Controller (VIC)

All internal and external interrupts are routed to the VIC, where hardware determines the interrupt priority (see Table 14). The VIC is also where the appropriate signal to the processor (IRQ or FIQ) is generated. The processor services the interrupt as either a vectored interrupt or a default-vectored interrupt.

The VIC accepts inputs from 32 interrupt source lines:

- Seven external
- Twenty-three internal
- Two used as software interrupts.

All 32 interrupt source lines can be enabled, disabled, and cleared individually, and individual status can be determined. On reset, all interrupts are disabled.

The VIC also accepts software-generated interrupts. Software-generated interrupts use the same enabling control as hardware-generated interrupts.

The VIC provides 32 interrupts:

- 16 vectored interrupts
- 16 or more default-vectored interrupts.

Any of the 32 interrupt source lines can be assigned to any of the 16 interrupt vectors. Any line not explicitly assigned to an interrupt vector is processed as a default-vectored interrupt. At reset, all 32 lines become default-vectored interrupts.

Each interrupt line can be explicitly identified as an IRQ (default) or FIQ interrupt. Vectored-interrupt servicing is only available for IRQ interrupts.

Table 14. Interrupt Channels

POSITION	DESCRIPTION	SOURCE
0	WDT	Watchdog Timer
1	Not Used	Available as a software interrupt
2	ARM7 DBGCOMMRX	Sourced by the ARM7TDMI-S Core
3	ARM7 DBGCOMMTX	Sourced by the ARM7TDMI-S Core
4	Timer0 Combined	Timer0
5	Timer1 Combined	Timer1
6	Timer2 Combined	Timer2
7	External Interrupt 0	Sourced by the GPIO Block
8	External Interrupt 1	Sourced by the GPIO Block
9	External Interrupt 2	Sourced by the GPIO Block
10	External Interrupt 3	Sourced by the GPIO Block
11	External Interrupt 4	Sourced by the GPIO Block
12	External Interrupt 5	Sourced by the GPIO Block
13	External Interrupt 6	Sourced by the GPIO Block
14	Not Used	Available as a software interrupt
15	RTC_ALARM	Real Time Clock
16	ADC TSCIRQ (combined)	Analog-to-Digital Converter
17	ADC BrownOutINTR	Brown Out Detector
18	ADC PenIRQ	Analog-to-Digital Converter
19	LCD	LCD Controller
20	SSPTXINTR	Synchronous Serial Port
21	SSPRXINTR	Synchronous Serial Port
22	SSPRORINTR	Synchronous Serial Port
23	SSPRXTOINTR	Synchronous Serial Port
24	SSPINTR	Synchronous Serial Port
25	UART1 UARTRXINTR	UART1
26	UART1 UARTTXINTR	UART1
27	UART1 UARTINTR	UART1
28	UART0 UARTINTR	UART0
29	UART2 Interrupt	UART2
30	DMA	DMA
31	CAN	CAN (LH75401/LH75400) Reserved (LH75411/LH75410)

Reset, Clock, and Power Controller (RCPC)

The RCPC lets users control System Reset, clocks, power management, and external interrupt conditioning via the AMBA APB interface. This control includes:

- Enabling and disabling various clocks
- Managing power-down sequencing
- Selecting the sources for various clocks.

The RCPC provides for an orderly start-up until the crystal oscillator stabilizes and the PLL acquires lock. If users want to change the system clock frequency during normal operation, the RCPC ensures a seamless transition between the old and new frequencies.

RCPC FEATURES

- Manages five Power Modes for minimizing power consumption: Active, Standby, Sleep, Stop1, and Stop2
- Generates the system clock (HCLK) from either the PLL clock or the PLL-bypassed (oscillator) clock, divided by 2, 4, 6, 8, … 30
- Generates three UART clocks from oscillator clock
- Generates the 1 Hz RTC clock
- Generates the SSP and LCD clocks from HCLK, divided by 1, 2, 4, 8, 16, 32, or 64
- Provides a selectable external clock output
- Generates system and RTC Resets based on an external reset, Watchdog Timer reset, or soft reset
- Configures seven HIGH/LOW-level or rising/falling edge-trigger external interrupts and converts them to HIGH-level trigger interrupt outputs required by the VIC
- Generates remap outputs used by the memory map decoder
- Provides an identification register
- Supports external or watchdog reset status.

Operating Modes

The LH75400/01/10/11 microcontrollers support three operating modes:

- Normal Mode
- PLL Bypass Mode, where the internal PLL is bypassed and an external clock source is used; otherwise the chip operates normally
- EmbeddedICE Mode, where the JTAG port accesses the TAP Controller in the core and the core is placed in Debug Mode.

The state of the TEST1, TEST2, and nRESETIN signals determines the operating mode entered at Power-on Reset (see Table 15).

Table 15. Device Operating Modes

OPERATING MODE	TEST2	TEST1	nRESETIN
Reserved	0	0	0
PLL Bypass	0	0	1
Reserved	0	1	x
Reserved	1	0	0
EmbeddedICE	1	0	1
Normal	1	1	x

NOTE: TEST1, TEST2, and nRESETIN are latched on the rising edge of nPOR. The microcontroller stays in that operating mode until power is removed or nPOR transitions from LOW to HIGH.

General Purpose Input/Output (GPIO)

The LH75400/01/10/11 microcontrollers have 10 GPIO ports:

- Seven 8-bit ports
- Two 7-bit ports
- One 6-bit port.

The GPIO ports are designated A through J and provide 76 bits of programmable input/output (see Table 16). Pins of all ports, except Port J, can be configured as inputs or outputs. Port J is input only. Upon System Reset, all ports default to inputs.

Table 16. GPIO Ports

PORT	PROGRAMMABLE PINS
A	8 Input/Output Pins
B	6 Input/Output Pins
C	8 Input/Output Pins
D	7 Input/Output Pins
E	8 Input/Output Pins
F	7 Input/Output Pins
G	8 Input/Output Pins
H	8 Input/Output Pins
I	8 Input/Output Pins
J	8 Input Pins

Device Pin Multiplexing

Table 17. LCD Panel Signal Multiplexing

EXTERNAL PIN	4-BIT STN (MONOCHROME)		8-BIT STN SINGLE PANEL (MONOCHROME)
	SINGLE PANEL	DUAL PANEL	
LVCVD11	Reserved	MLSTN3	Reserved
LVCVD10	Reserved	MLSTN2	Reserved
LVCVD9	Reserved	MLSTN1	Reserved
LVCVD8	Reserved	MLSTN0	Reserved
LVCVD7	Reserved	Reserved	MUSTN7
LVCVD6	Reserved	Reserved	MUSTN6
LVCVD5	Reserved	Reserved	MUSTN5
LVCVD4	Reserved	Reserved	MUSTN4
LVCVD3	MUSTN3	MUSTN3	MUSTN3
LVCVD2	MUSTN2	MUSTN2	MUSTN2
LVCVD1	MUSTN1	MUSTN1	MUSTN1
LVCVD0	MUSTN0	MUSTN0	MUSTN0

NOTES:
1. MUSTN = Mono upper panel STN, dual and/or single panel.
2. MLSTN = Mono lower panel STN, dual panel only.

Table 18. LCD External Pin Multiplexing (LH75401 and LH75411)

EXTERNAL PIN	DEFAULT MODE (NO LCD)	4-BIT MONO STN MODE		8-BIT STN MODE	TFT MODE	ALI MODE
		SINGLE	DUAL			
PG4/LCDVEEEN/LCDMOD	PG4	LCDVEEEN	LCDVEEEN	LCDVEEEN	LCDVEEEN	LCDMOD
PG3/LCDVDDEN	PG3	LCDVDDEN	LCDVDDEN	LCDVDDEN	LCDVDDEN	LCDVDDEN
PG2/LCDDSPLEN/LCDREV	PG2	LCDDSPLEN	LCDDSPLEN	LCDDSPLEN	LCDDSPLEN	LCDREV
PG1/LCDCLS	PG1	PG1	PG1	PG1	PG1	LCDCLS
PG0/LCDPS	PG0	PG0	PG0	PG0	PG0	LCDPS
PH7/LCDDCLK	PH7	LCDDCLK	LCDDCLK	LCDDCLK	LCDDCLK	LCDDCLK
PH6/LCDLP/LCDHRLP	PH6	LCDLP	LCDLP	LCDLP	LCDLP	LCDLP
PH5/LCDFP/LCDSPS	PH5	LCDFP	LCDFP	LCDFP	LCDFP	LCDFP
PH4/LCDEN/LCDEN	PH4	LCDEN	LCDEN	LCDEN	LCDEN	LCDEN
PH3/LCDVD11	PH3	PH3	MLSTN3	PH3	LCDVD11	LCDVD11
PH2/LCDVD10	PH2	PH2	MLSTN2	PH2	LCDVD10	LCDVD10
PH1/LCDVD9	PH1	PH1	MLSTN1	PH1	LCDVD9	LCDVD9
PH0/LCDVD8	PH0	PH0	MLSTN0	PH0	LCDVD8	LCDVD8
PI7/LCDVD7	PI7	PI7	PI7	STN7	LCDVD7	LCDVD7
PI6/LCDVD6	PI6	PI6	PI6	STN6	LCDVD6	LCDVD6
PI5/LCDVD5	PI5	PI5	PI5	STN5	LCDVD5	LCDVD5
PI4/LCDVD4	PI4	PI4	PI4	STN4	LCDVD4	LCDVD4
PI3/LCDVD3	PI3	MUSTN3	MUSTN3	STN3	LCDVD3	LCDVD3
PI2/LCDVD2	PI2	MUSTN2	MUSTN2	STN2	LCDVD2	LCDVD2
PI1/LCDVD1	PI1	MUSTN1	MUSTN1	STN1	LCDVD1	LCDVD1
PI0/LCDVD0	PI0	MUSTN0	MUSTN0	STN0	LCDVD0	LCDVD0

Table 19. LCD External Pin Multiplexing (LH75400 and LH75410)

EXTERNAL PIN	DEFAULT MODE (NO LCD)	4-BIT MONO STN MODE		8-BIT MONO STN MODE
		SINGLE	DUAL	
PG4/LCDVEEEN	PG4	LCDVEEEN	LCDVEEEN	LCDVEEEN
PG3/LCDVDDEN	PG3	LCDVDDEN	LCDVDDEN	LCDVDDEN
PG2/LCDDSPLEN	PG2	LCDDSPLEN	LCDDSPLEN	LCDDSPLEN
PG1	PG1	PG1	PG1	PG1
PG0	PG0	PG0	PG0	PG0
PH7/LCDDCLK	PH7	LCDDCLK	LCDDCLK	LCDDCLK
PH6/LCDLP	PH6	LCDLP	LCDLP	LCDLP
PH5/LCDFP	PH5	LCDFP	LCDFP	LCDFP
PH4/LCDEN	PH4	LCDEN	LCDEN	LCDEN
PH3/LCDVD11	PH3	PH3	MLSTN3	PH3
PH2/LCDVD10	PH2	PH2	MLSTN2	PH2
PH1/LCDVD9	PH1	PH1	MLSTN1	PH1
PH0/LCDVD8	PH0	PH0	MLSTN0	PH0
PI7/LCDVD7	PI7	PI7	PI7	MUSTN7
PI6/LCDVD6	PI6	PI6	PI6	MUSTN6
PI5/LCDVD5	PI5	PI5	PI5	MUSTN5
PI4/LCDVD4	PI4	PI4	PI4	MUSTN4
PI3/LCDVD3	PI3	MUSTN3	MUSTN3	MUSTN3
PI2/LCDVD2	PI2	MUSTN2	MUSTN2	MUSTN2
PI1/LCDVD1	PI1	MUSTN1	MUSTN1	MUSTN1
PI0/LCDVD0	PI0	MUSTN0	MUSTN0	MUSTN0

ELECTRICAL SPECIFICATIONS

Table 20. Absolute Maximum Ratings

PARAMETER	MINIMUM	MAXIMUM
DC Core Supply Voltage (VDDC)	-0.3 V	2.4 V
DC I/O Supply Voltage (VDD)	-0.3 V	4.6 V
DC Analog Supply Voltage for ADC (VDDA0)	-0.3 V	4.6 V
DC Analog Supply Voltage for PLL (VDDA1)	-0.3 V	2.4 V
Storage Temperature (TSTG)	-55°C	125°C

NOTE: These ratings are only for transient conditions. Operation at or beyond absolute maximum rating conditions may affect reliability and cause permanent damage to the device.

Table 21. Recommended Operating Conditions

PARAMETER	MINIMUM	TYP.	MAXIMUM	NOTES
DC Core Supply Voltage (VDDC) (Linear Regulator disabled)	1.7 V	1.8 V	1.98 V	1
DC Analog Supply Voltage for ADC (VDDA0)	3.0 V	3.3 V	3.6 V	
DC I/O Supply Voltage (VDD)	3.0 V	3.3 V	3.6 V	1
DC Analog Supply Voltage for PLL (VDDA1)	1.7 V	1.8 V	1.98 V	2
Clock Frequency (fHCLK)	4.375 MHz		84 MHz	3, 4, 5
Clock Period (tHCLK)	11.9047 ns		228.571 ns	3, 4, 5
Crystal Frequency	14 MHz		20 MHz	4, 5
Industrial Operating Temperature	-40°C	25°C	85°C	

NOTES:
1. Core Voltage should never exceed I/O Voltage after initial power up. See the section titled ‘Power Supply Sequencing’.
2. Connect VDDA1 to VDDC when using the on-chip linear regulator.
3. On-chip Linear regulator enabled. When the on-chip linear regulator is enabled, Core power is drawn from VDD – allow VDDC pins to float.
4. Will operate to DC with PLL disabled. Core frequencies greater than 84 MHz require external clock and VDDC.
5. Processor is functional at minimum frequency, but not all peripherals may be enabled.
6. The maximum operating frequency is the crystal frequency × 3.5.

Table 22. Clock Frequency vs. Voltages (VDD) vs. Temperature

PARAMETER		1.7 V	1.8 V	1.9 V
25°C	Clock Frequency (fHCLK)	91.3 MHz	97 MHz	103.7 MHz
	Clock Period (tHCLK)	10.952 ns	10.309 ns	9.643 ns
70°C	Clock Frequency (fHCLK)	86 MHz	92 MHz	97.4 MHz
	Clock Period (tHCLK)	11.627 ns	10.869 ns	10.266 ns
85°C	Clock Frequency (fHCLK)	84 MHz	90 MHz	95.2 MHz
	Clock Period (tHCLK)	11.9047 ns	11.111 ns	10.504 ns

NOTES:
1. On-chip Linear regulator and PLL disabled; VDDC supplied externally.
2. Core speeds greater than 84 MHz require external VDDC and may not yield proper UART baud rates.
3. Additional performance may be achieved in accordance with Figure 10.

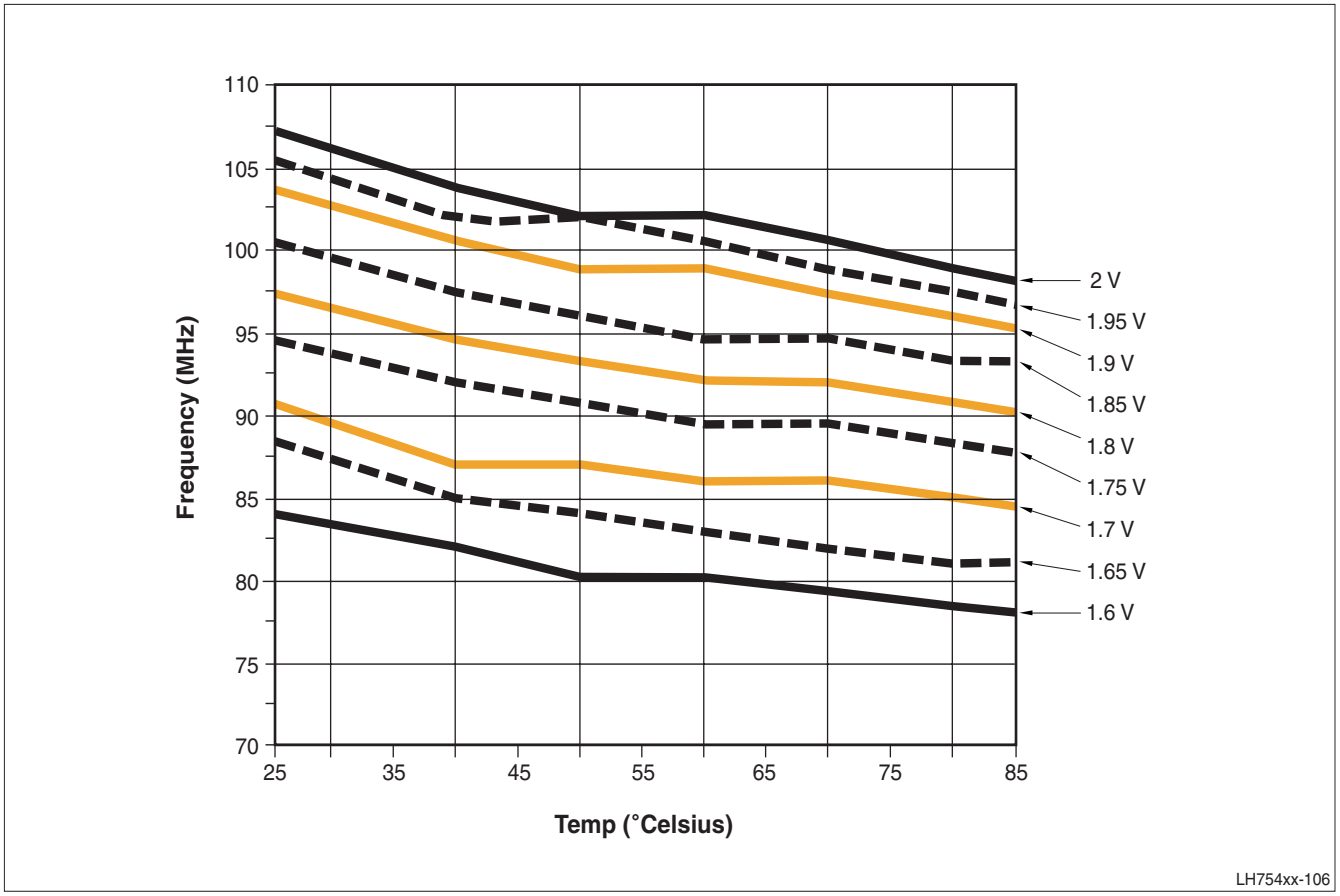


Figure 10. Maximum Core Frequency versus Voltage and Temperature

Very Low Operating Temperatures and Noise Immunity

The junction temperature, Tj, is the operating temperature of the transistors in the integrated circuit. The switching speed of the CMOS circuitry within the SoC depends partly on Tj, and the lower the operating temperature, the faster the CMOS circuits will switch. Increased switching noise generated by faster switching circuits could affect the overall system stability. The amount of switching noise is directly affected by the application executed on the SoC.

SHARP recommends that users implementing a system to meet low industrial temperature standards should use an external oscillator rather than a crystal to drive the system clock input of the System-on-Chip. This change from crystal to oscillator will increase the robustness (ie, noise immunity of the clock input to the SoC.

DC Characteristics

All characteristics are specified over an operating temperature of -40°C to +85°C, and at minimum and maximum supply voltages.

Table 23. DC Characteristics

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	CONDITIONS	NOTES
VIH	CMOS Input HIGH Voltage	2.0			V		
VIL	CMOS Input LOW Voltage			0.8	V		1
VT+	Schmitt Trigger Positive Going Threshold	2.0			V		
VT-	Schmitt Trigger Negative Going Threshold			0.8	V		
Vhst	Schmitt Trigger Hysteresis	0.35			V		
VOH	Output Drive 1	2.6			V	IOH = -2 mA	
	Output Drive 2	2.6			V	IOH = -4 mA	
	Output Drive 3	2.6			V	IOH = -6 mA	
	Output Drive 4	2.6			V	IOH = -8 mA	
VOL	Output Drive 1			0.4	V	IOL = 2 mA	
	Output Drive 2			0.4	V	IOL = 4 mA	
	Output Drive 3			0.4	V	IOL = 6 mA	
	Output Drive 4			0.4	V	IOL = 8 mA	
XTAL32IN	External Clock Input	1.62	1.8	1.98	V	Externally supplied	
XTALIN	External Clock Input	1.62	1.8	1.98	V	Externally supplied	
IIN	Input Leakage Current	-10		10	µA	VIN = VDD or GND	
IACTIVE	Active Current		50	70	mA		2
ISTANDBY	Standby Current		45		mA		2
ISLEEP	Sleep Current		4.0		mA		
ISTOP1	Stop1 Current		3.0		mA		
ISTOP2	Stop2 Current (RTC ON)		35		µA		3
			120		µA		4
ISTOP2	Stop2 Current (RTC OFF)		23		µA		3
			100		µA		4

NOTES:
1. VIL MAX. = 0.5 V for pin TCK with 50 pF load.
2. Running a Typical Application at 51.6 MHz.
3. Using external 1.8 V supply, internal regulator disabled.
4. Using Internal linear regulator.

Table 24. Linear Regulator DC Characteristics

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
IQUIESCENT	Quiescent Current		75		µA
ISLEEPLR	Current when Regulator is Disabled		8		µA
IOLR	Output Current Range	0.0		100	mA
VOLR	Output Voltage		1.84		V
RPULL	Pull-up Resistor			0	Ω

Analog-To-Digital Converter Electrical Characteristics

Table 25 shows the derated specifications for extended temperature operation. See Figure 11 for the ADC transfer characteristics.

Table 25. ADC Electrical Characteristics at Industrial Operating Range

PARAMETER	MIN.	TYP.	MAX.	UNITS	NOTES
A/D Resolution	10		10	Bits	
Throughput Conversion	17			CLK Cycles	1
Acquisition Time	3			CLK Cycles	
Clk Frequency	500		5,000	ns	
Differential Non-Linearity	-0.99		4.5	LSB	
Integral Non-Linearity	-3.5		+3.5	LSB	
Offset Error	-35		+35	mV	
Gain Error	-4.0		4.0	LSB	
On-chip Voltage Reference (VREF)	1.85	2.0	2.15	V	
Negative Reference Input (VREF-)	VSSA	VSSA	(VREF+) -1.0	V	2
Positive Reference Input (VREF+)	(VREF-) +1.0	VREF	VDDA	V	2
Crosstalk between channels		-60		dB	
Analog Input Voltage Range	0		VDDA	V	3
Analog Input Current			5	µA	
Reference Input Current			5	µA	
Analog input capacitance			15	pF	
Operating Supply Voltage	3.0		3.6	V	
Operating Current, VDDA		590		µA	
Standby Current		180		µA	4
Stop Current, VDDA		< 1		µA	
Brown Out Trip Point		2.63		V	
Brown Out Hysterisis		120		mV	
Operating Temperature	-40		85	°C	

NOTES:

1. The analog section of the ADC takes 16 × A2DCLK cycles per conversion, plus 1 × A2DCLK cycles to be made available in the PCLK domain. An additional 3 × PCLK cycles are required before being available on the APB.
2. The internal voltage reference is driven to nominal value VREF = 2.0 V. Using the Reference Multiplexer, alternative low impedance (RS < 500) voltages can be selected as reference voltages. The range of voltages allowed are specified above. However, the on-chip reference cannot drive the ADC unless the reference buffer is switched on.
3. The analog input pins can be driven anywhere between the power supply rails. If the voltage at the input to the ADC exceeds VREF+ or is below VREF-, the A/D result will saturate appropriately at positive or negative full scale. Trying to pull the analog input pins above or below the power supply rails will cause protection diodes to be forward-biased, resulting in large current source/sink and possible damage to the ADC.
4. Bandgap and other low-bandwidth circuitry operating. All other ADC blocks shut down.

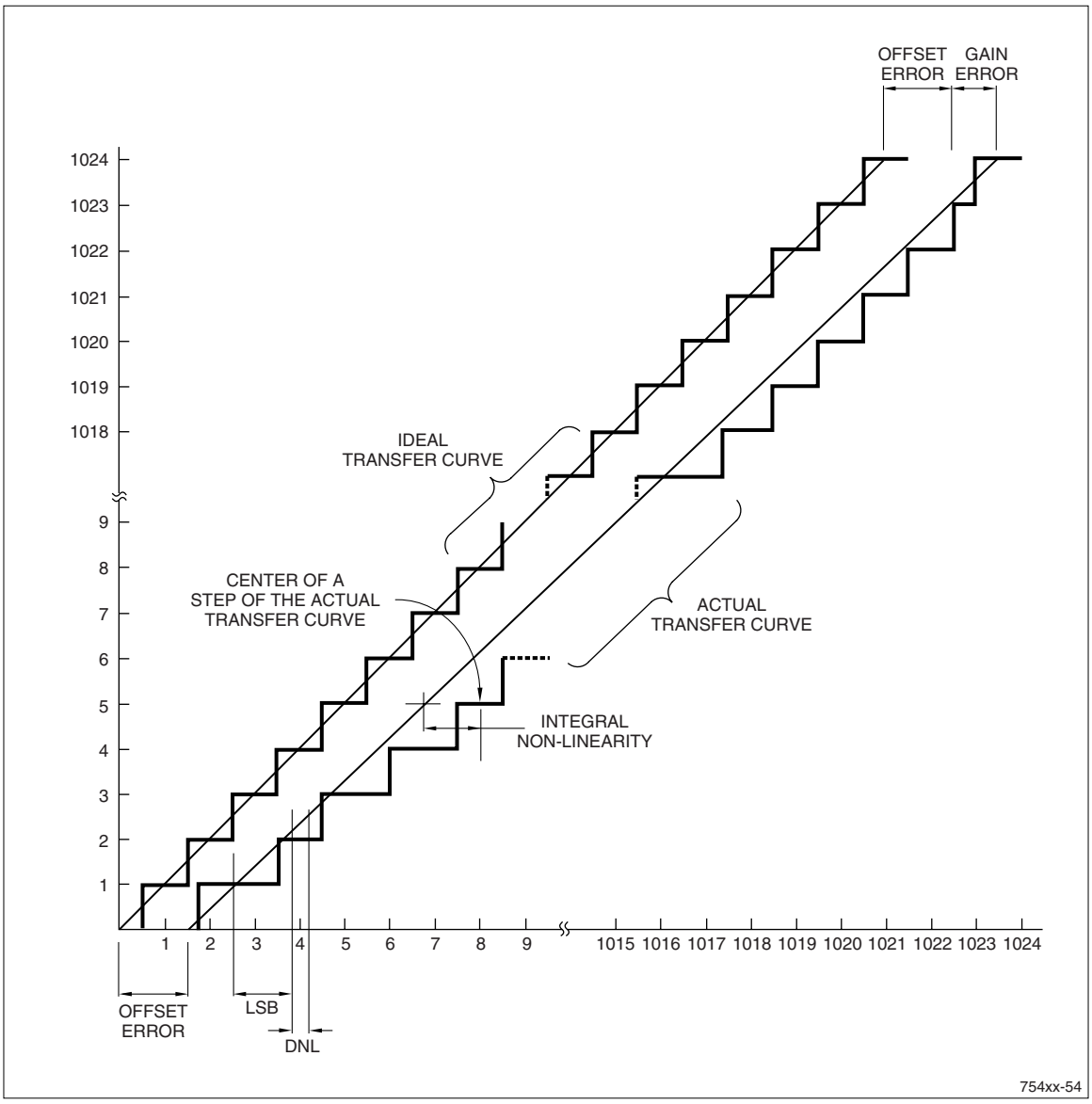


Figure 11. ADC Transfer Characteristics

POWER SUPPLY SEQUENCING

When using an external 1.8 V supply (instead of the internal 1.8 V regulator), the external 1.8 V power supply must be energized before the 3.3 V supply. Otherwise, the 1.8 V supply may not lag the 3.3 V supply by more than 10 µs.

If a longer delay time is needed, the voltage difference between the two power supplies must be within 1.5 V during power supply ramp up.

To avoid a potential latchup condition, voltage should be applied to input pins only after the device is powered-on as described above.

LINEAR REGULATOR

Although this device contains an on-board regulator, using its output to power external devices is not recommended. External loads can affect the regulator's stability and introduce noise into the supply. SHARP cannot guarantee device performance at rated speeds and temperatures with external loads connected to this supply.

CURRENT CONSUMPTION BY OPERATING MODE

Current consumption can depend on a number of parameters. To make this data more usable, the values presented in Table 26 were derived under the conditions presented here.

Maximum Specified Value

The values specified in the MAXIMUM column were determined using these operating characteristics:

- All IP blocks either operating or enabled at maximum frequency and size configuration
- Core operating at maximum power configuration
- All I/O loads at maximum (50 pF)
- All voltages at maximum specified values
- Maximum specified ambient temperature.

Typical

The values in the TYPICAL column were determined using a 'typical' application under 'typical' environmental conditions and the following operating characteristics:

- SPI, Timer, and UART peripherals operating; all other peripherals disabled
- LCD enabled with 320 × 240 × 16-bit color, 60 Hz refresh rate
- I/O loads at nominal
- FCLK = 51.6 MHz; HCLK = 51.6 MHz
- All voltages at typical values
- Nominal case temperature.

PERIPHERAL CURRENT CONSUMPTION

In addition to the modal current consumption, Table 27 shows the typical current consumption for each of the on-board peripheral blocks. The values were determined with the peripheral clock running at maximum frequency, typical conditions, and no I/O loads. This current is supplied by the 1.8 V power supply.

Table 26. Current Consumption by Mode

SYMBOL	PARAMETER	TYP.	UNITS
ACTIVE MODE			
ICHIP	Chip Current with Linear Regulator	50.2	mA
ICORE	Core Current without Linear Regulator	42.1	mA
IIO	I/O Current without Linear Regulator	5	mA
IANALOG	Analog Current	1.3	mA
STANDBY MODE (TYPICAL CONDITIONS ONLY)			
ICHIP	Core Current with Linear Regulator	42.7	mA
ICORE	Core Current without Linear Regulator	34.6	mA
IIO	Current drawn by I/O	0.8	mA
IANALOG	Analog Current	1.3	mA
SLEEP MODE (TYPICAL CONDITIONS ONLY)			
ICHIP	Core Current with Linear Regulator	3.9	mA
ICORE	Core Current without Linear Regulator	2.5	mA
IIO	Current drawn by I/O	400	µA
IANALOG	Analog Current	1.2	mA
STOP1 MODE			
ISTOP	Core Current with Linear Regulator, I/O, and 14.7456 MHz osc.	2.96	mA
STOP2 MODE (RTC ON)			
ILEAK	Leakage Current, Core and I/O	34	µA
STOP2 MODE (RTC OFF)			
ILEAK	Leakage Current, Core and I/O	18	µA

NOTES:
1. ICHIP = Chip Current with Linear Regulator (Core + I/O)
2. ICORE, IIO, IANALOG are the respective current consumption specifications for VDDC, VDD, and VDDA.

Table 27. Peripheral Current Consumption

PERIPHERAL	TYPICAL	UNITS
UARTs	200	µA
RTC	5	µA
DMA	4.1	mA
SSP	500	µA
Counter/Timers	200	µA
LCD	2.2	mA

AC Characteristics

All signal transitions are measured from the 50% point of the signal.

Table 28. Memory Interface Signals

SIGNAL	I/O	LOAD	PARAMETER	MINIMUM	MAXIMUM	COMMENTS
D[15:0]	Out	50 pF	tOVD		tHCLK + 8 ns	Data output valid following address valid
D[15:0]	Out	50 pF	tOHD	3 × tHCLK – 6 ns		Data output invalid following address valid
D[15:0]	In		tIDD		2 tHCLK – 18 ns	Data input valid following address valid
					2 × tHCLK – 18 ns + (nWAIT –1) × tHCLK	Data Input Valid, following Address Valid (nWAIT states)
nCS3 - nCS0	Out	30 pF	tOVCS		tHCLK + 6 ns	nCS output valid following address valid
nCS3 -nCS0	Out	30 pF	tOHCS	3 × tHCLK – 6 ns		nCS output invalid following address valid
nOE	Out	30 pF	tOVOE		tHCLK + 10 ns	nOE output valid following address valid
nOE	Out	30 pF	tOHOE	3 × tHCLK – 6 ns		nOE output invalid following address valid
nBLE1 - nBLE0	Out	30 pF	tOVBE		tHCLK + 10 ns	nBLE output valid following address valid
nBLE1 - nBLE0	Out	30 pF	tOHBER	3 × tHCLK – 6 ns		nBLE output invalid following address valid, read cycle
nBLE1 - nBLE0	Out	30 pF	tOHBEW	2 × tHCLK – 6 ns		nBLE output invalid following address valid, write cycle
nWE	Out	30 pF	tOVWE		tHCLK + 10 ns	nWE output valid following address valid
nWE	Out	30 pF	tOHWE	2 × tHCLK – 6 ns	2 tHCLK – 2.2 ns	nWE output invalid following address valid
nWAIT	In		tIVWAIT		2 tHCLK – 18 ns	nWAIT input valid following address valid

NOTE: The values in Table 28 represent the timing with no internal arbitration delay and 1 wait state memory access. This is the worst case (fastest) timing.

Table 29. Synchronous Serial Port

SIGNAL	I/O	LOAD	PARAMETER	MIN.	MAX.	COMMENT
SSPFRM	Out	50 pF	tOVSSPFRM		14 ns	SSPFRM output valid, referenced to SSPCLK
SSPTX	Out	50 pF	tOVSSPTX		12 ns	SSPTX output valid, referenced to SSPCLK
SSPRX	In		tISSPRX	22 ns		SSPRX input valid, referenced to SSPCLK

Table 30. Power-up Stabilization

PARAMETER	DESCRIPTION	TYP.	MAX.	UNIT
tLREG	Linear regulator stabilization time after power-up		200	µs
tOSC32	Oscillator stabilization time after Power Up (VDDC = VDDCMIN)		550	ms
tOSC14	Oscillator stabilization time after Power Up (VDDC = VDDCMIN)		2.5	ms
tRSTOV	nPOR LOW to nPOR valid (once sampled LOW)	3.5		HCLK
tPORH	nPOR hold extend to allow PLL to lock once XTAL is stable		10	µs

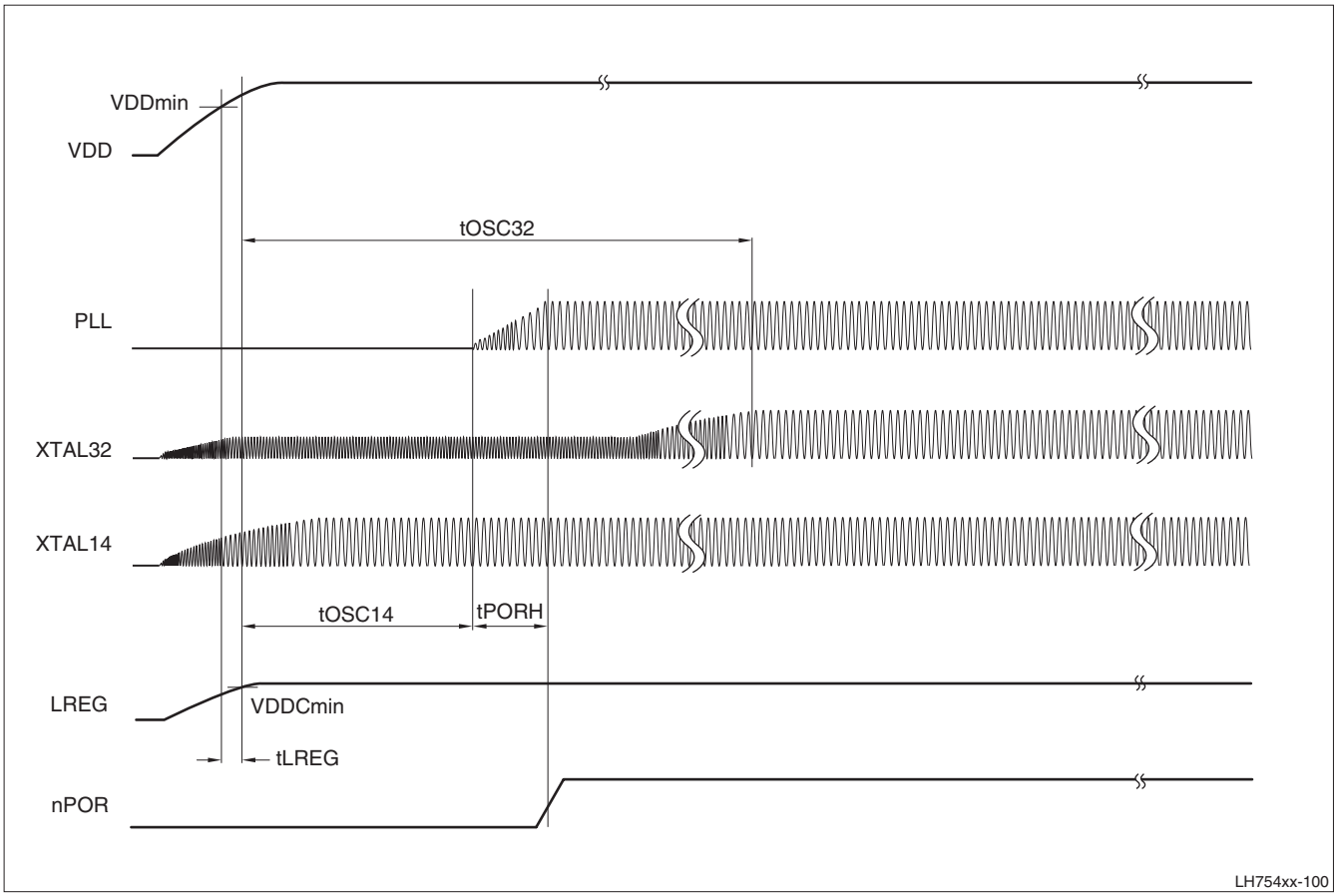


Figure 12. Power-up Stabilization

MEMORY CONTROLLER WAVEFORMS

Static Memory Controller Waveforms

Figure 13 shows the waveform and timing for an External Static Memory Write, with one Wait State. Figure 14 shows the waveform and timing for an External Static Memory Write, with two Wait States. Figure 15 shows the waveform and timing for an External Static Memory Read, with one Wait State.

The SMC supports an nWAIT input that can be used by an external device to extend the wait time during a memory access. The SMC samples nWAIT at the beginning of at the beginning of each system clock cycle. The system clock cycle in which the nCSx signal is asserted counts as the first wait state. See Figure 16. The SMC recognizes that nWAIT is active within 2 clock cycles after it has been asserted. To assure that the current access (read or write) will be extended by nWAIT, program at least two wait states for this bank of memory. If N wait states are programmed, the SMC holds this state for N system clocks or until the SMC detects that nWAIT is inactive, whichever occurs last. As the number of wait states programmed increases, the amount of delay before nWAIT must be asserted also increases. If only 2 wait states are programmed, nWAIT must be asserted in the clock cycle immediately following the clock cycle during which the nCSx signal is asserted. Once the SMC detects that the external device has deactivated nWAIT, the SMC completes its access in 3 system clock cycles.

The formula for the allowable delay between asserting nCSx and asserting nWAIT is:

tASSERT = (system clock period) × (Wait States - 1)
(where Wait States is from 2 to 31.)

The signal tIDD is shown without a setup time, as measurements are made from the Address Valid point and HCLK is an internal signal, shown for reference only.

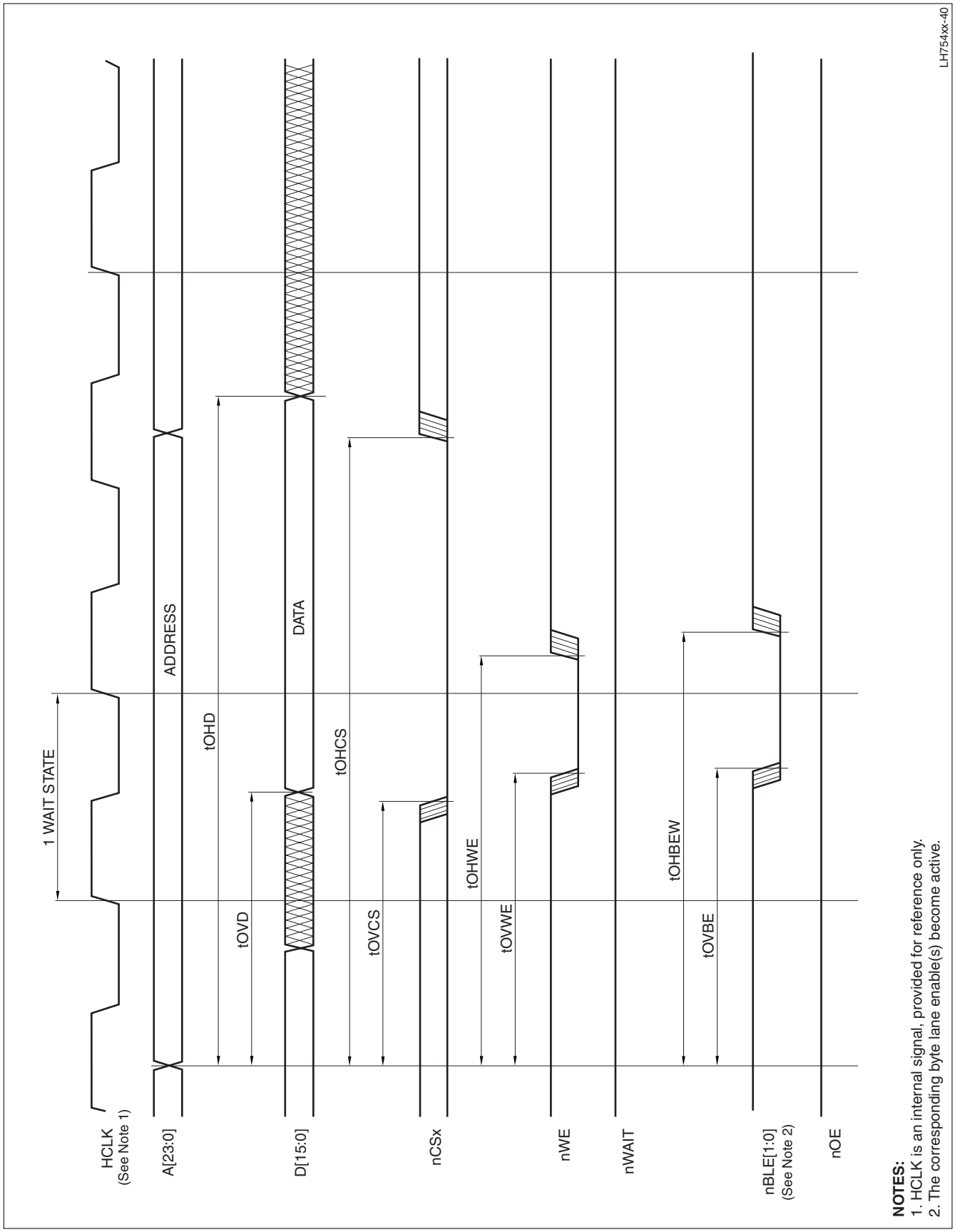


Figure 13. External Static Memory Write, One Wait State

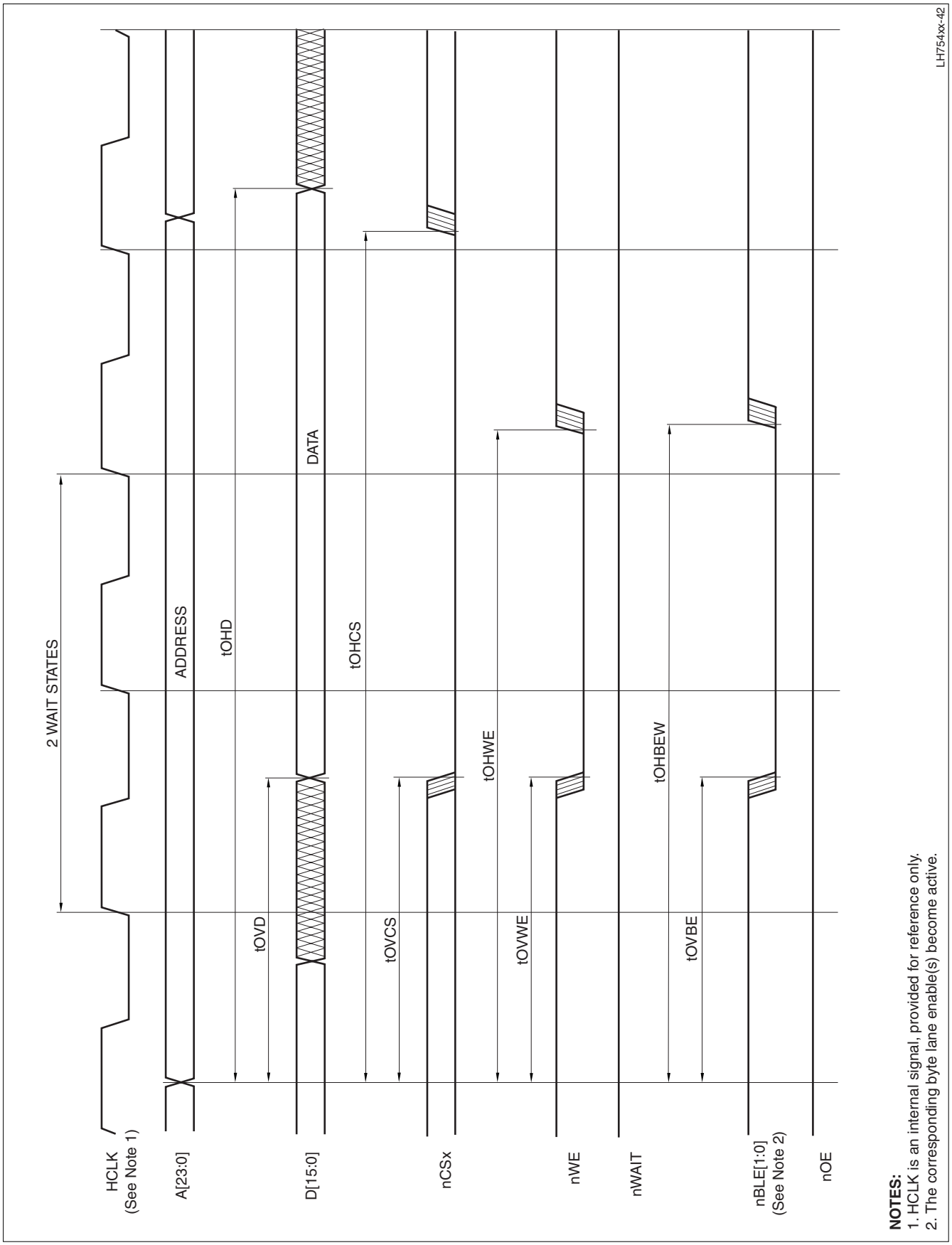


Figure 14. External Static Memory Write, Two Wait States

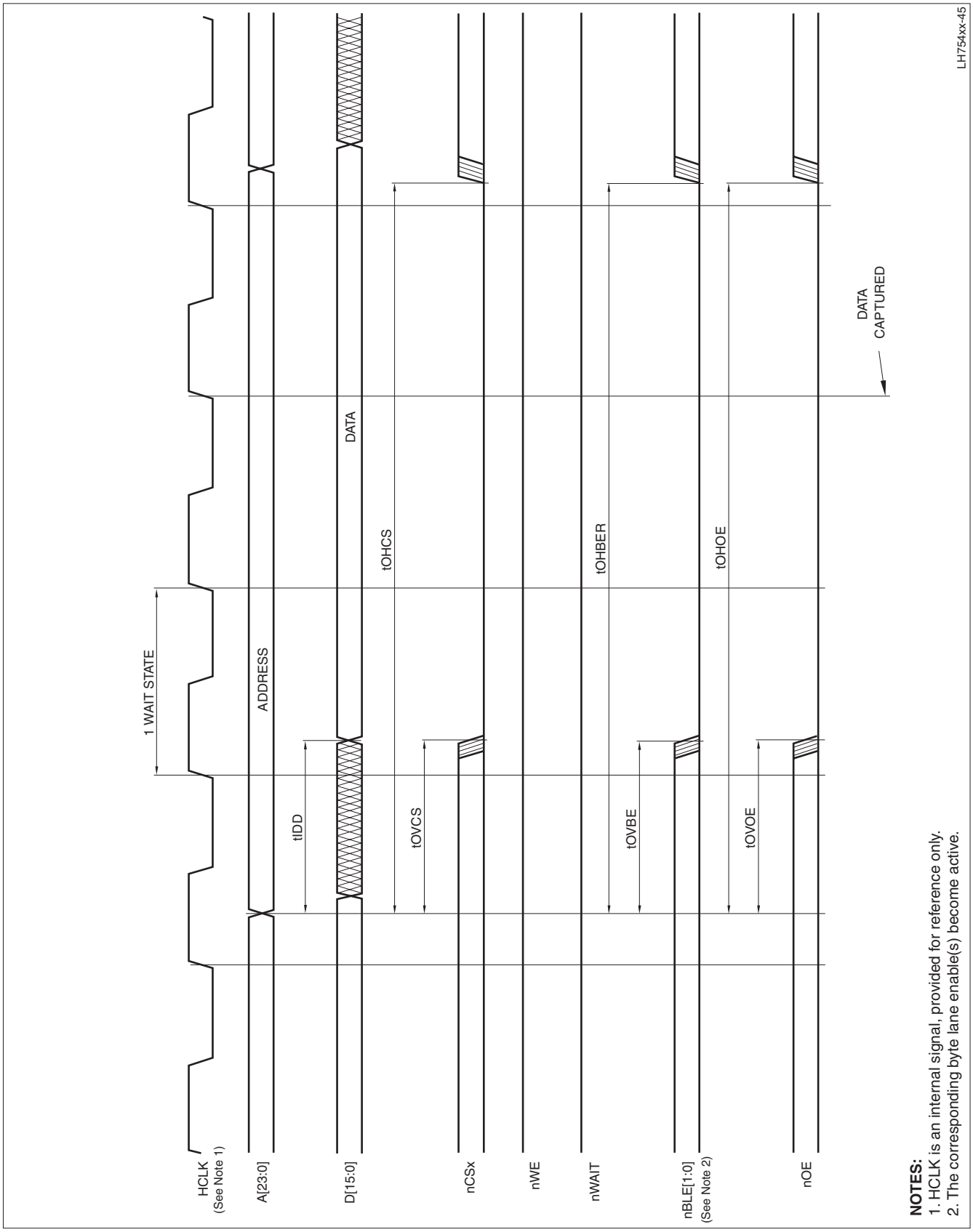


Figure 15. External Static Memory Read, One Wait State

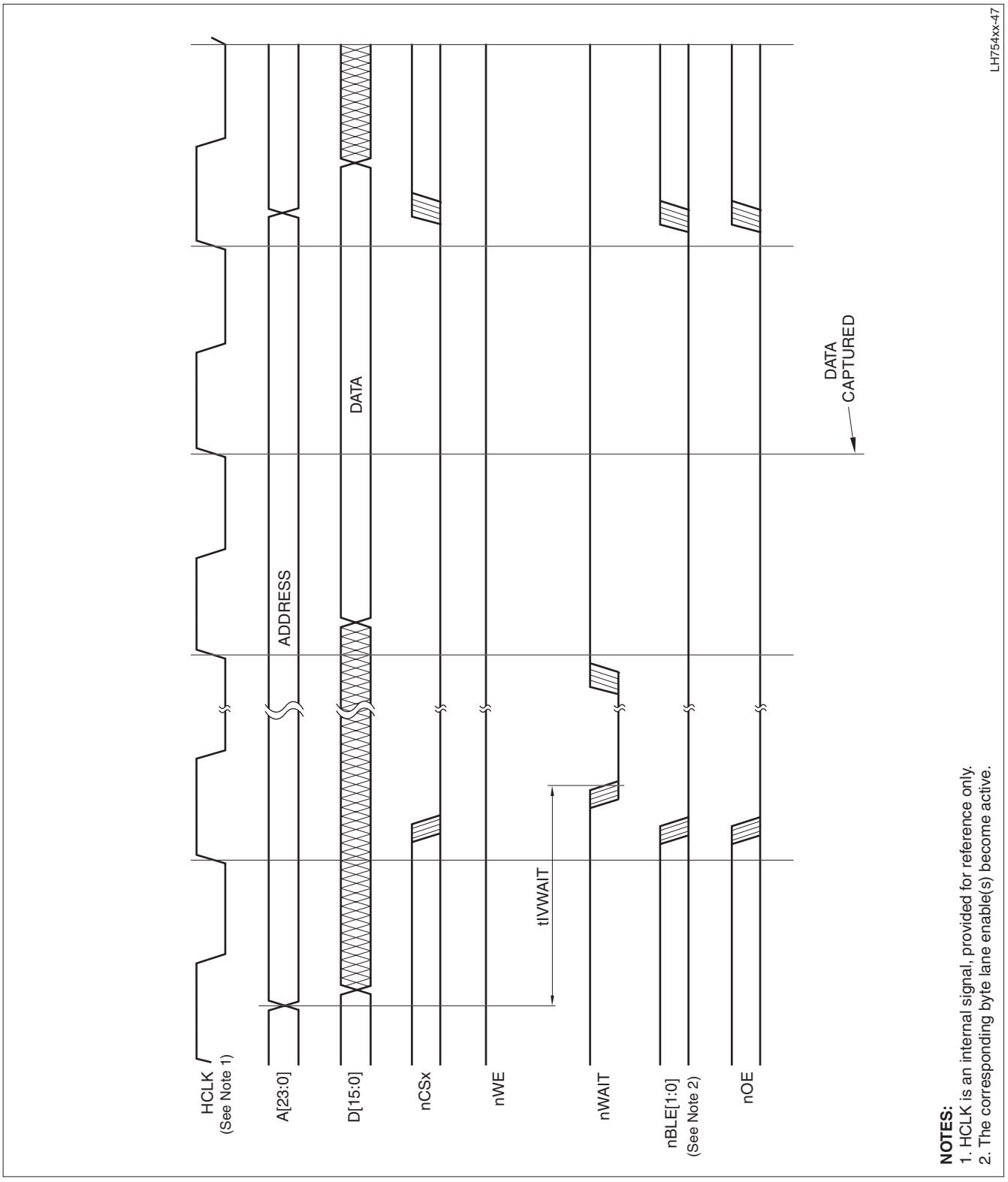


Figure 16. External Static Memory Read, nWAIT Active

Synchronous Serial Port Waveform

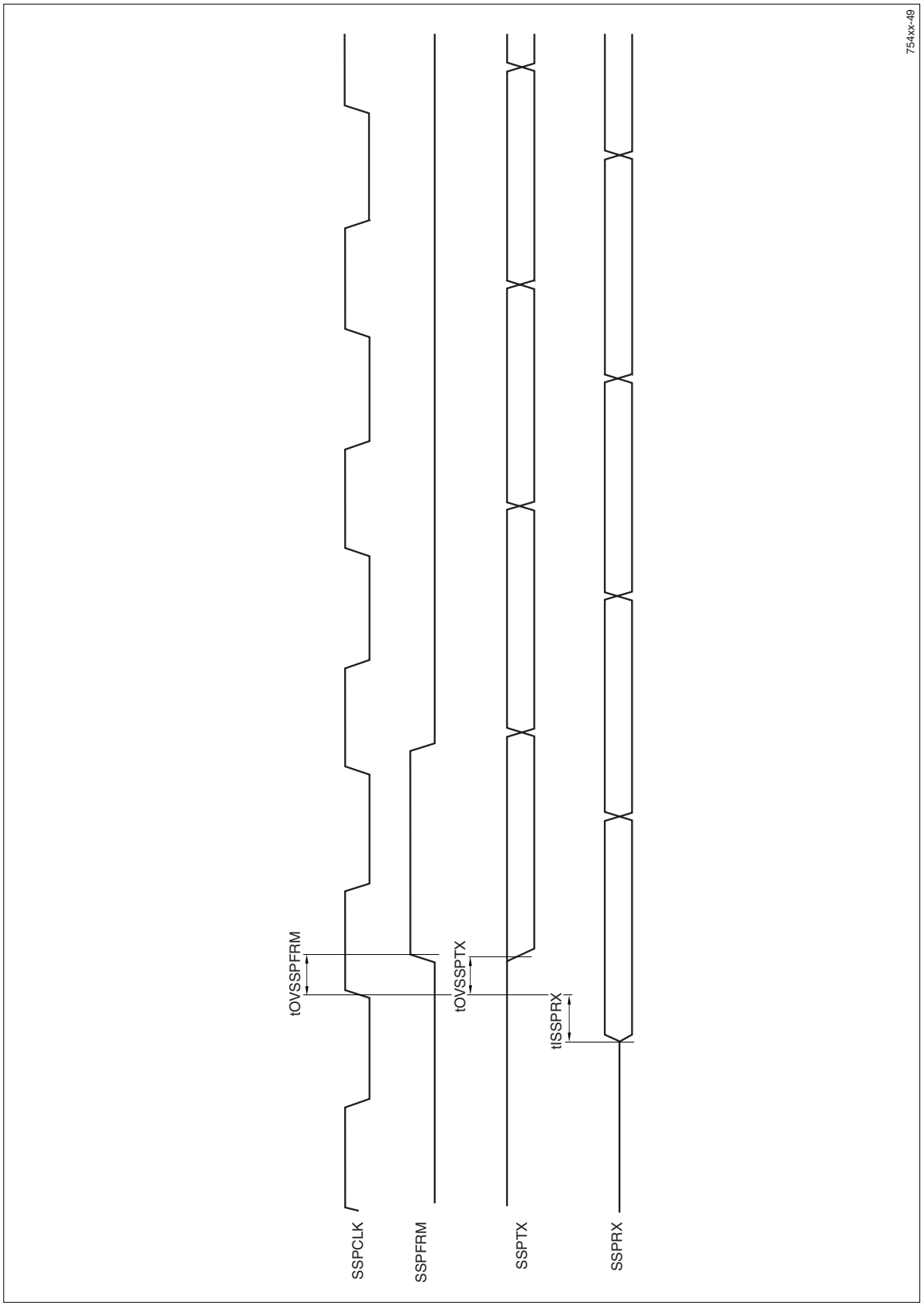


Figure 17. Synchronous Serial Port Waveform

DMA Controller Timing Diagrams

Figure 18 and Figure 19 show examples of DMA timing diagrams.

- Figure 18 shows the timing for a peripheral-to-memory data transfer, where SoSize = DeSize and SoBurst = 4.
- Figure 19 shows the timing for a memory-to-peripheral data transfer, where SoSize = DeSize and SoBurst = 4.

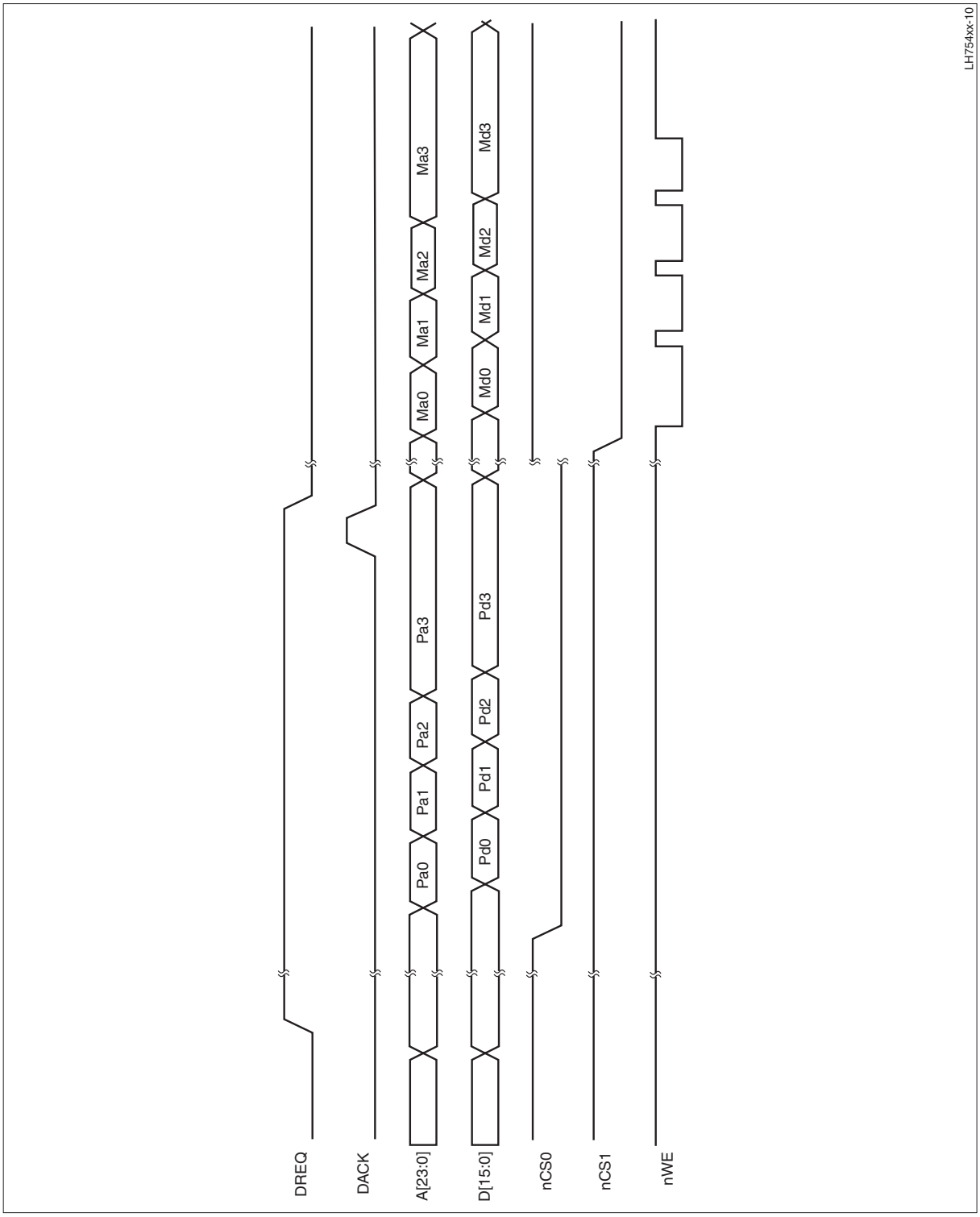


Figure 18. Peripheral-to-Memory Data-Transfer Timing

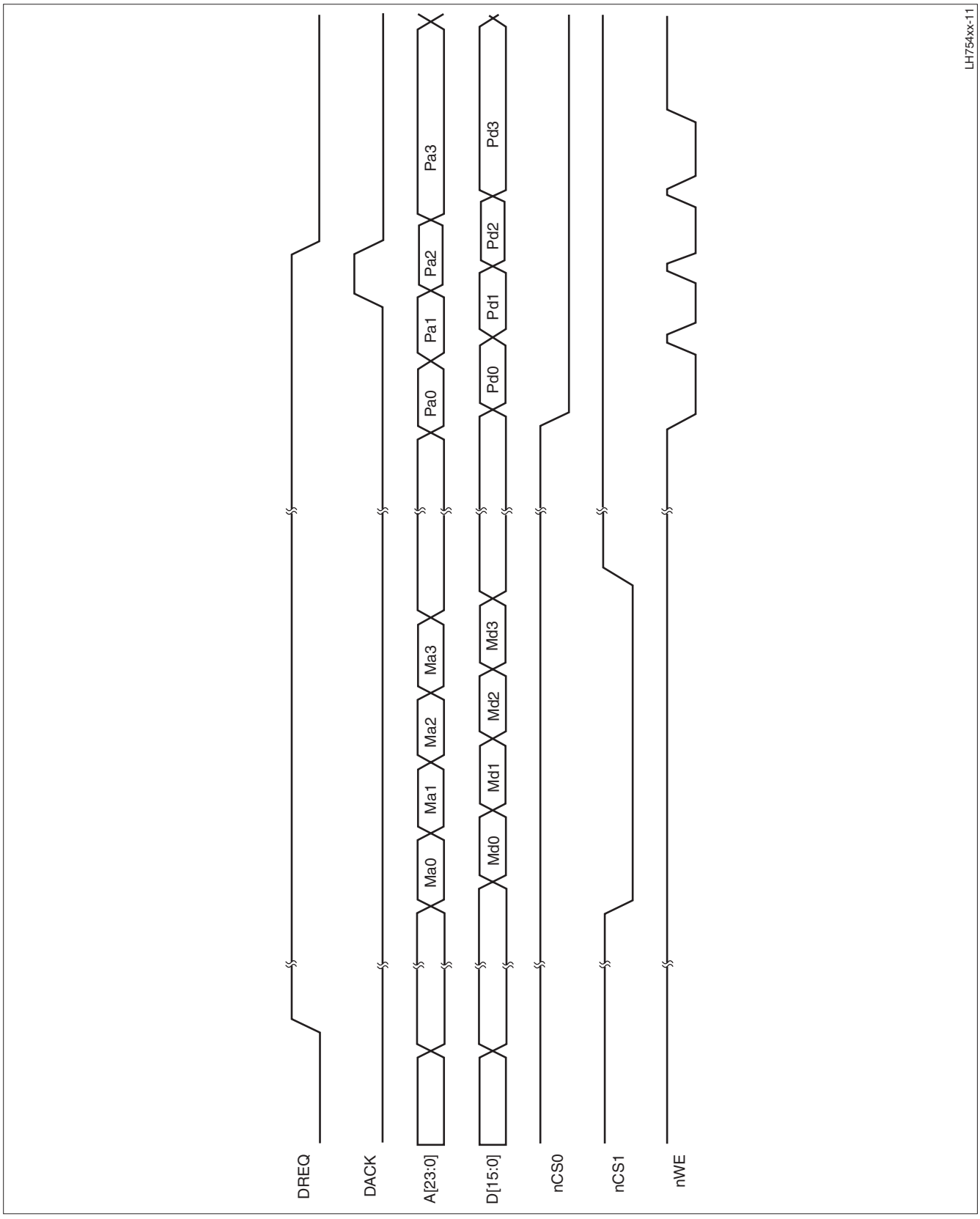


Figure 19. Memory-to-Peripheral Data-Transfer Timing

Color LCD Controller Timing Waveforms

This section describes typical output waveform diagrams for the CLCDC and the Advanced LCD Interface.

STN HORIZONTAL TIMING

Figure 20 shows typical horizontal timing waveforms for STN panels. In this figure, the CLCDC Clock (an input to the CLCDC) is scaled within the CLCDC and used to produce the LCDDCLK output. Programmable registers in the CLCDC set the timings (in terms of LCDDCLK pulses) to produce the other signals that control an STN display.

For example, Figure 20 shows that the duration of the LCDLP signal is controlled by Timing0:HSW (the HSW bit field in the Timing0 Register). Figure 20 also shows that the polarity of the LCDLP signal is set by Timing2:IHS.

STN VERTICAL TIMING

Figure 21 shows typical vertical timing waveforms for STN panels.

TFT HORIZONTAL TIMING

Figure 22 shows typical horizontal timing waveforms for TFT panels.

TFT VERTICAL TIMING

Figure 23 shows typical vertical timing waveforms for TFT panels.

AD-TFT/HR-TFT HORIZONTAL TIMING WAVEFORMS

Figure 24 shows typical horizontal timing waveforms for AD-TFT and HR-TFT panels. The ALI adjusts the normal TFT timing to accommodate these panels.

AD-TFT/HR-TFT VERTICAL TIMING WAVEFORMS

Figure 25 shows typical vertical timing waveforms for AD-TFT and HR-TFT panels. The power sequencing and register information is the same as for TFT vertical timing.

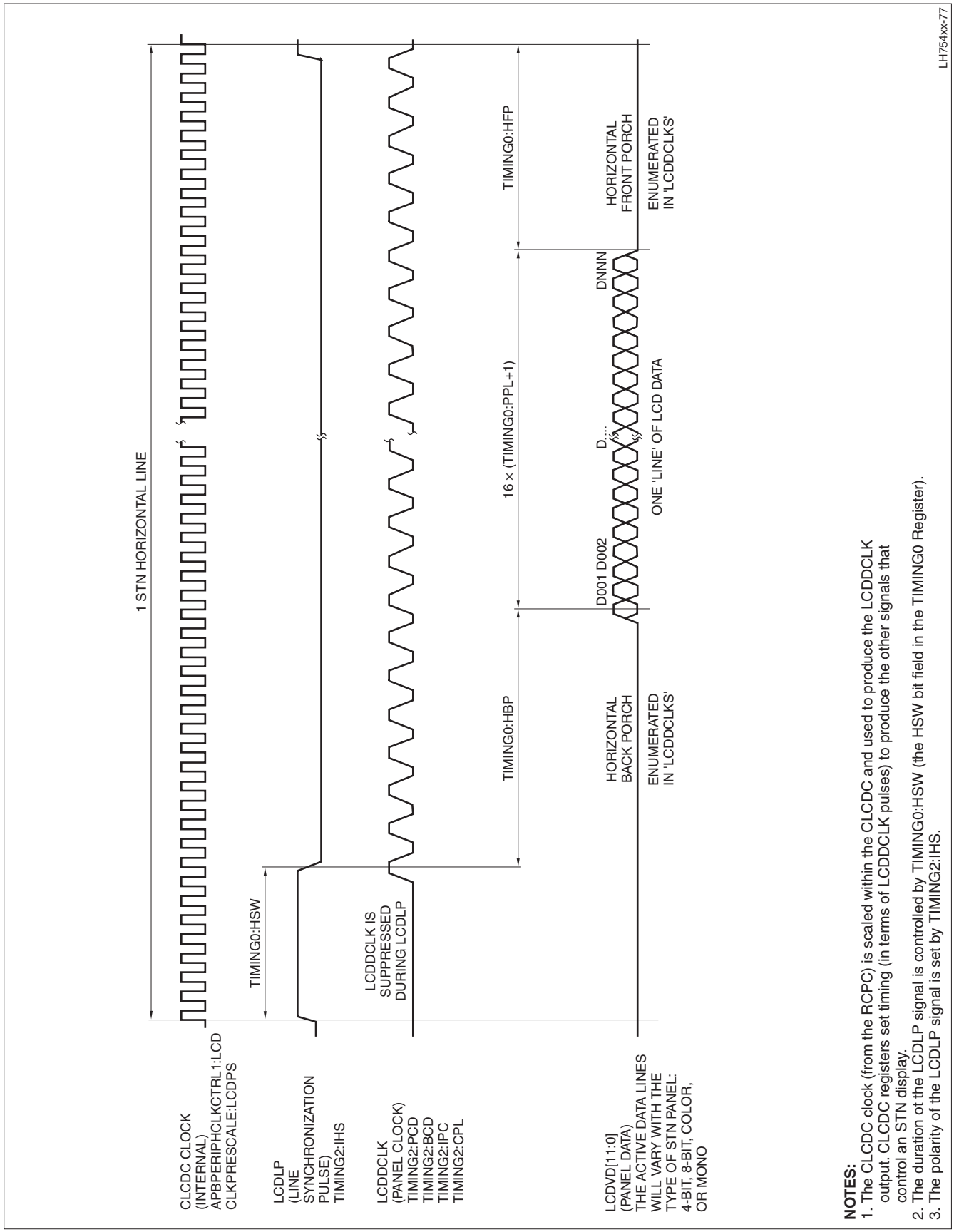


Figure 20. STN Horizontal Timing Diagram

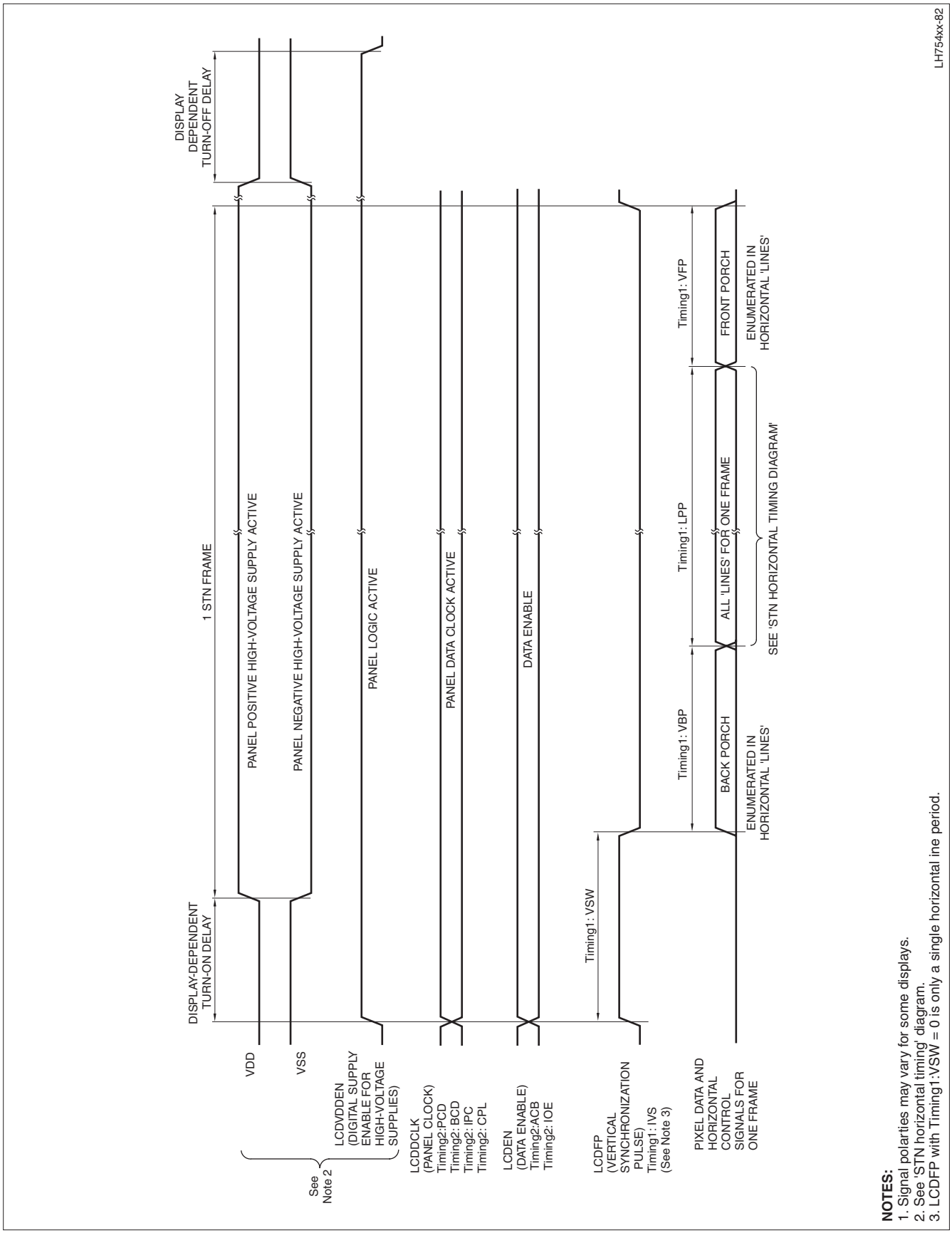


Figure 21. STN Vertical Timing Diagram

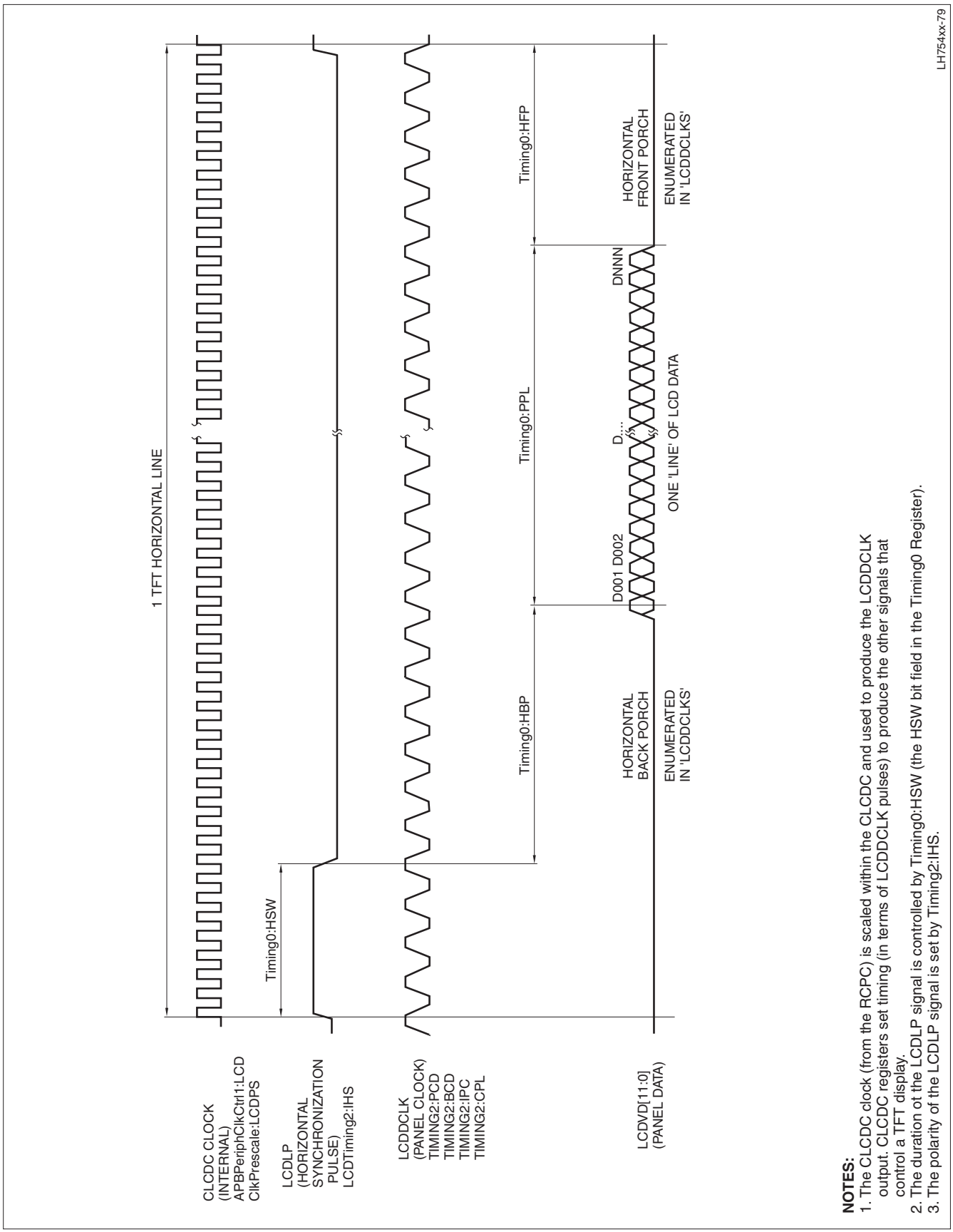


Figure 22. TFT Horizontal Timing Diagram

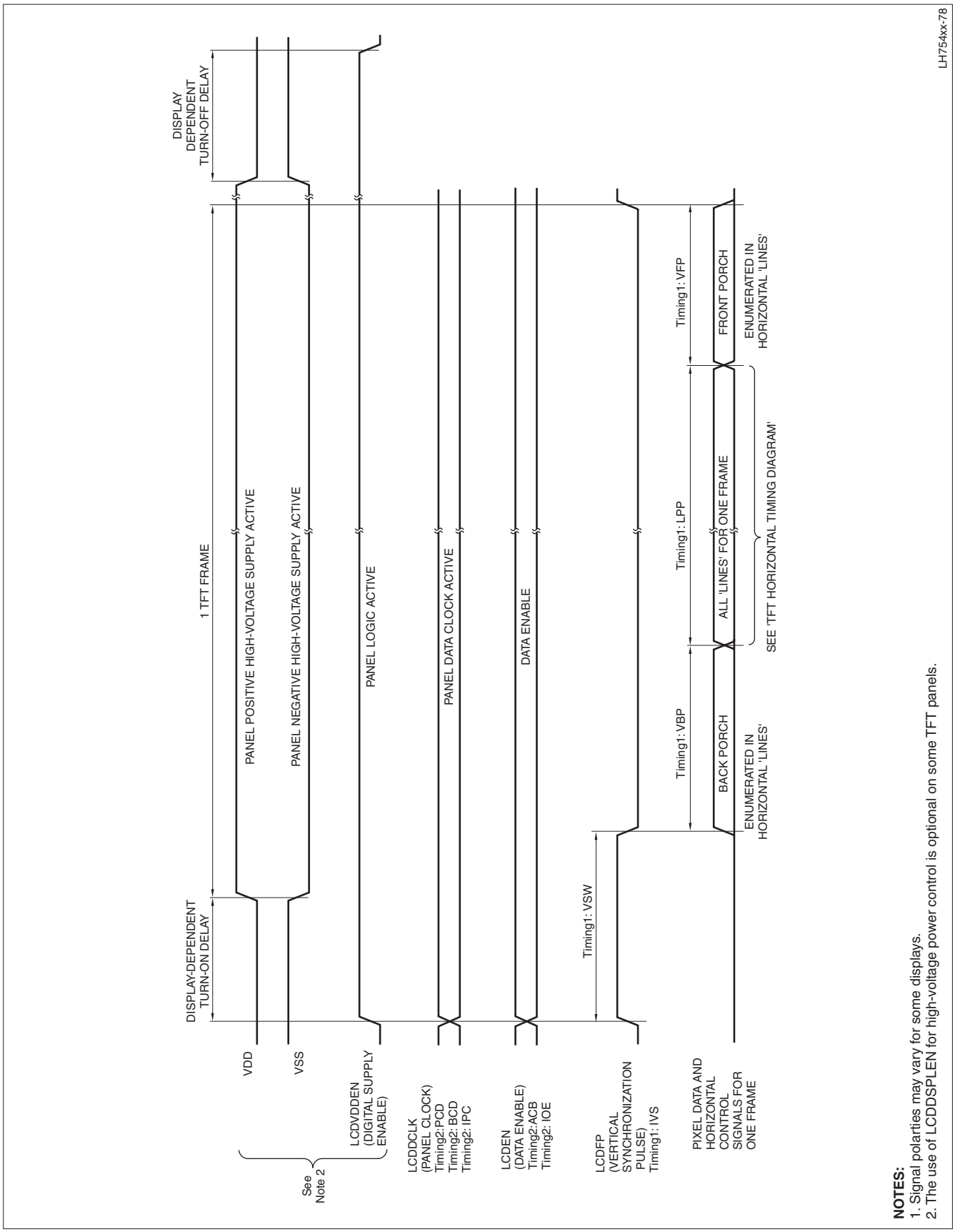


Figure 23. TFT Vertical Timing Diagram

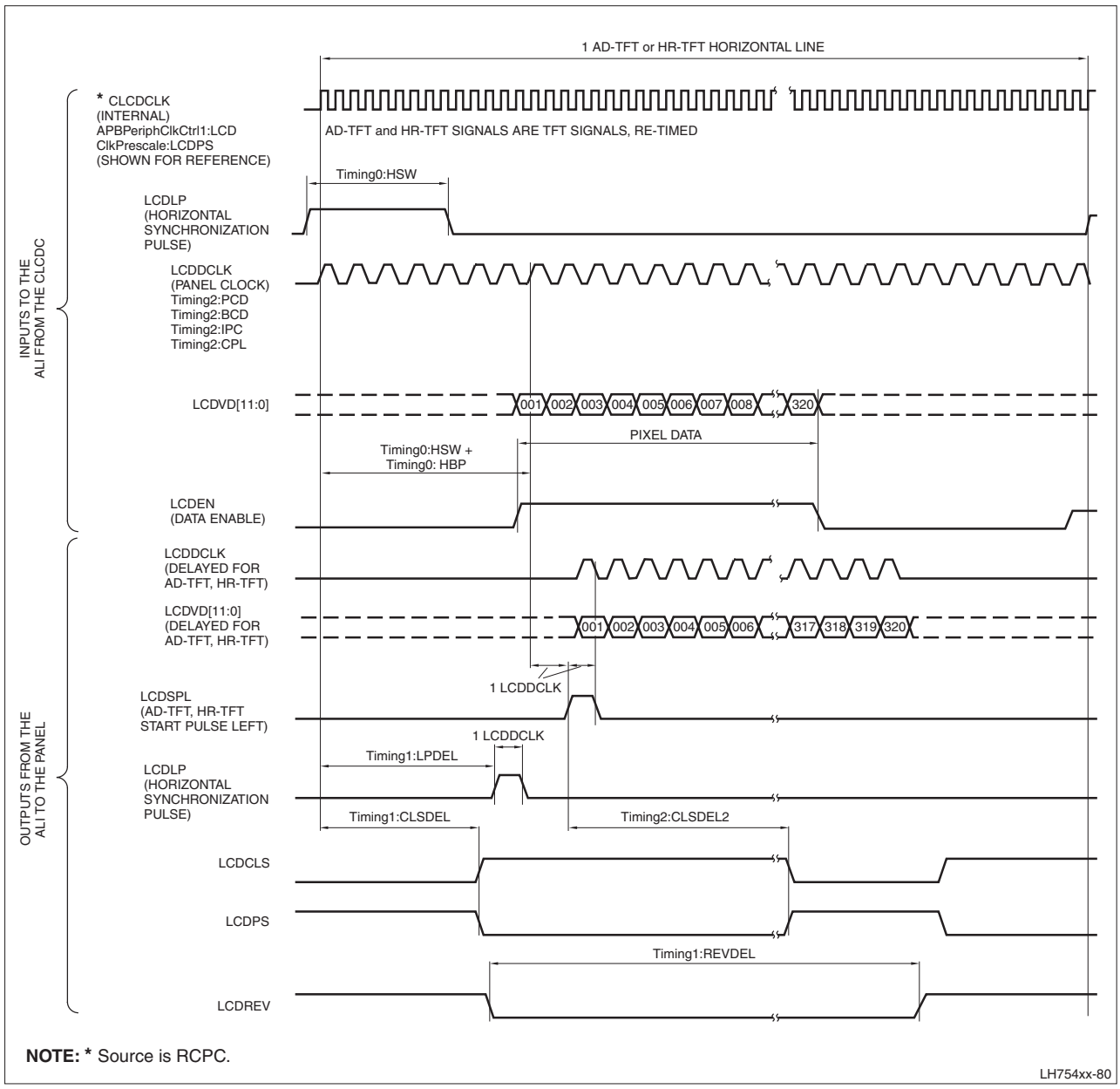


Figure 24. AD-TFT, HR-TFT Horizontal Timing Diagram

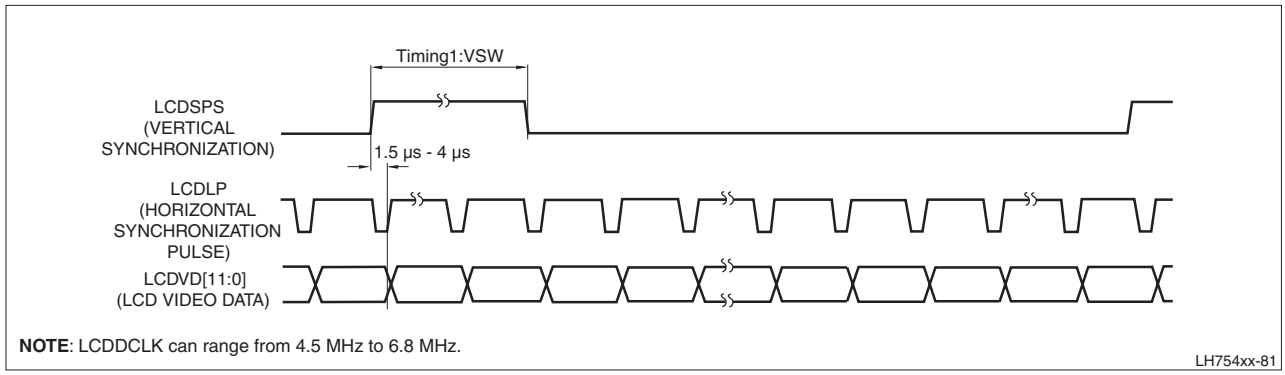
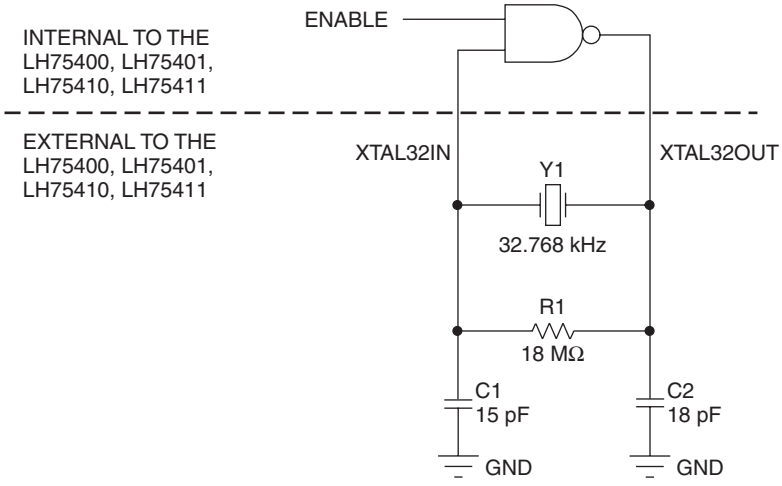


Figure 25. AD-TFT, HR-TFT Vertical Timing Diagram

SUGGESTED EXTERNAL COMPONENTS

Figure 26 shows the suggested external components for the 32.768 kHz crystal circuit to be used with the SHARP LH75400/01/10/11. The NAND gate represents the logic inside the SoC. See the chart for crystal specifics.

Figure 27 shows the suggested external components for the 14.7456 MHz crystal circuit to be used with the SHARP LH75400/01/10/11. The NAND gate represents the logic inside the SoC. See the chart for crystal specifics.



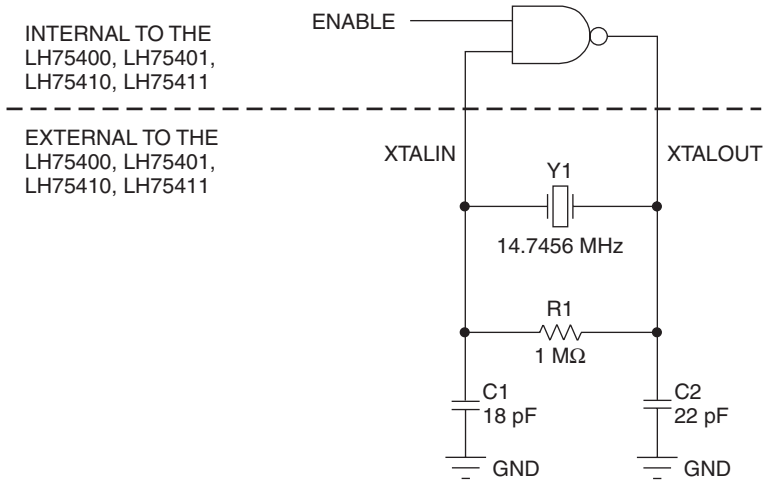
NOTES:
1. Y1 is a parallel-resonant type crystal. (See table)
2. The nominal values for C1 and C2 shown are for a crystal specified at 12.5 pF load capacitance (CL).
3. The values for C1 and C2 are dependent upon the cystal's specified load capacitance and PCB stray capacitance.
4. R1 must be in the circuit.
5. Ground connections should be short and return to the ground plane which is connected to the processor's core ground pins.
6. Tolerance for R1, C1, C2 is ≤ 5%.

RECOMMENDED CRYSTAL SPECIFICATIONS

PARAMETER	DESCRIPTION
32.768 kHz Crystal	Parallel Mode
Tolerance	±30 ppm
Aging	±3 ppm
Load Capacitance	12.5 pF
ESR (MAX.)	50 kΩ
Drive Level	1.0 µW (MAX.)
Recommended Part	MTRON SX1555 or equivalent

LH754xx-101

Figure 26. Suggested External Components, 32.768 kHz Oscillator



NOTES:
1. Y1 is a parallel-resonant type crystal. (See table)
2. The nominal values for C1 and C2 shown are for a crystal specified at 18 pF load capacitance (CL).
3. The values for C1 and C2 are dependent upon the cystal's specified load capacitance and PCB stray capacitance.
4. R1 must be in the circuit.
5. Ground connections should be short and return to the ground plane which is connected to the processor's core ground pins.
6. Tolerance for R1, C1, C2 is ≤ 5%.

RECOMMENDED CRYSTAL SPECIFICATIONS

PARAMETER	DESCRIPTION
14.7456 MHz Crystal	(AT-Cut) Parallel Mode
Tolerance	±50 ppm
Stability	±100 ppm
Aging	±5 ppm
Load Capacitance	18 pF
ESR (MAX.)	40 Ω
Drive Level	100 µW (MAX.)
Recommended Part	MTRON SX2050 or equivalent

LH754xx-102

Figure 27. Suggested External Components, 14.7456 MHz Oscillator

PACKAGE SPECIFICATIONS

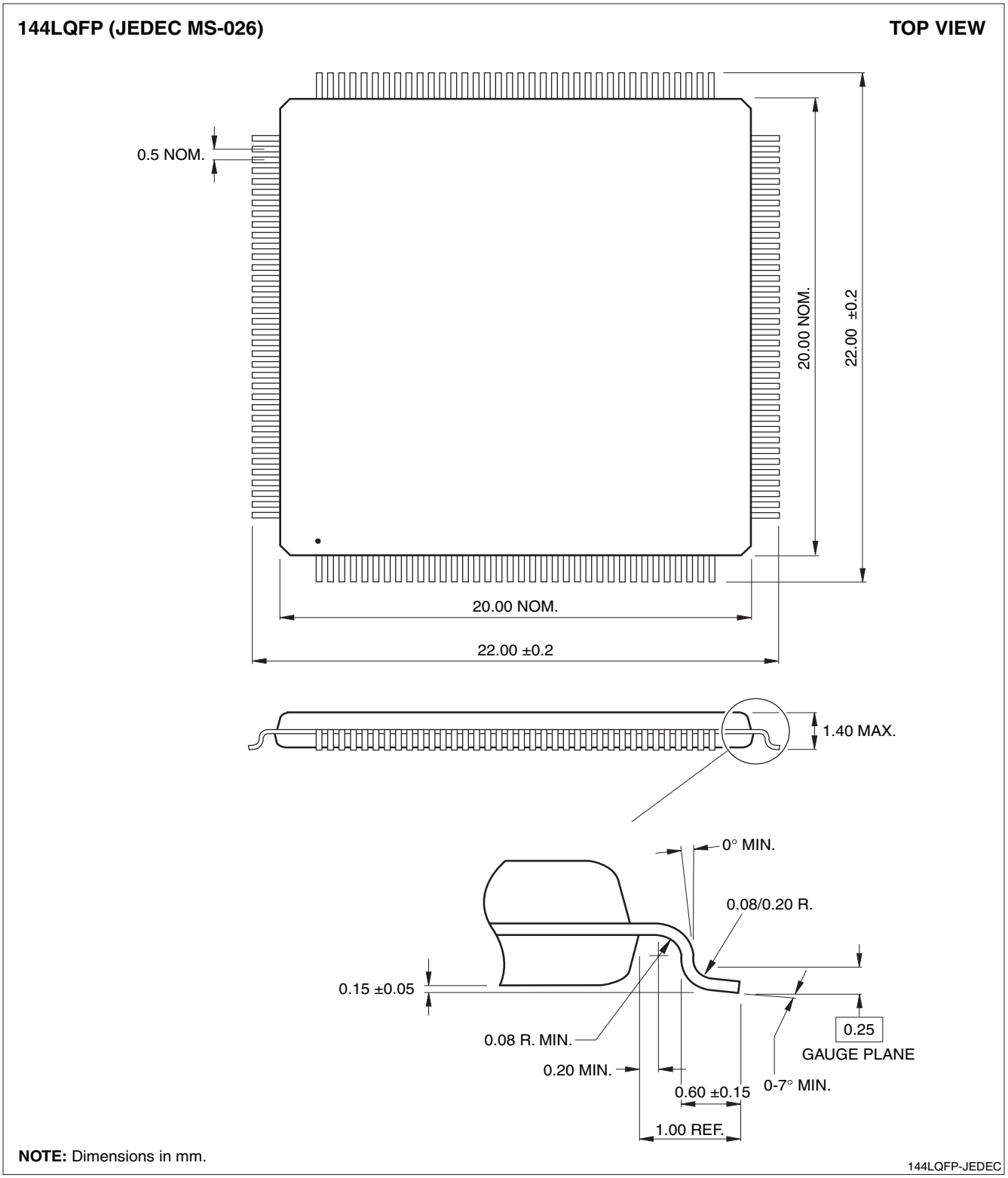
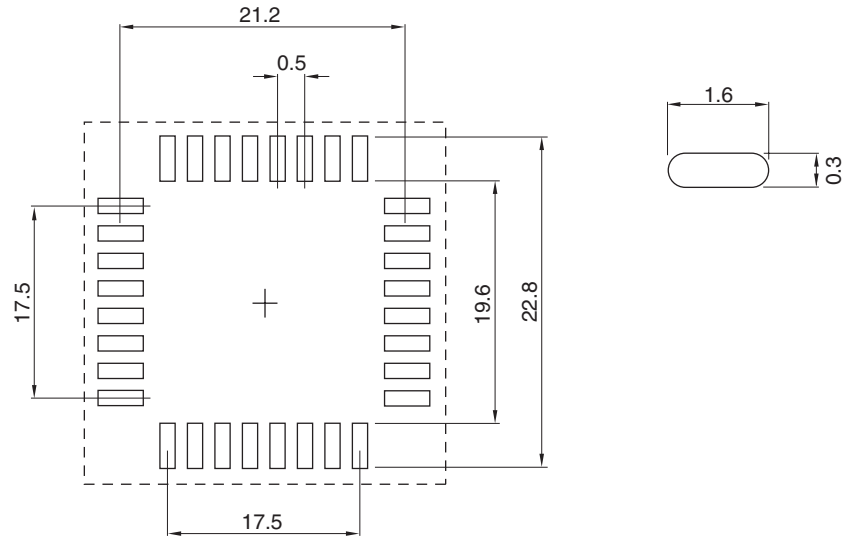


Figure 28. 144-pin LQFP

144LQFP



NOTE: Dimensions in mm.

144LQFP

Figure 29. Recommended PCB Footprint

CONTENT REVISIONS

This document contains the following changes to content, causing it to differ from previous versions.

Table 31. Record of Revisions

DATE	PAGE NO.	PARAGRAPH OR ILLUSTRATION	SUMMARY OF CHANGES
5-14-04	—		'Preliminary' Status removed.
	1	—	Core Speed Specification and Crystal Specifications updated.
	1	Page Note	Tolerance of XTAL inputs noted.
	8 - 10, 18 - 20, 28 - 30,	Tables 1, 3, 5, 7	Column heading for Reset behavior clarified; memory interface lines behavior during Reset clarified; notes added regarding voltage tolerance of XTAL inputs, need for 10 kΩ pull-up resistor to activate the on-chip linear regulator; SSPFRM and SSPCLK signals type corrected to Output.
	12, 22, 49	AD-TFT, HR-TFT Interface description	Corrected to Advanced LCD Interface description, text updated for clarity.
	46	Clock Sources	Rewritten to reflect updated specifications
	58	Table 22	DC Characteristics of XTAL inputs added.
		Table 23	Pull-up resistor for Linear Regulator specified.
	61	Table 27	Start-up Characteristics Table expanded.
	62	Current Consumption	Current Consumption by Operating Mode added.
	64	Figure 11	Start-up Characteristics Figure expanded.
	69, 70	Figures 18, 19	Suggested External Components added.
	73	Figure 21	Recommended PCB Footprint added.
05-20-05	—	—	Version number rolled to 1.1.
	10, 20, 30, 40, 59	Table Notes Table Notes Table 24	Pull-up resistor value for Linear Regulator updated.
	51	SSP Features	Text regarding interrupt-driven transfers clarified.
	72	Figure 20	Specification Drawing updated to add clearance under chip.
03-30-06	—	—	Version number rolled to 1.2.
	1	Features	Top Speed adjusted to reflect MAX. Temp and MIN. Voltage
	1	Pin Drawings	Note added to refer to device Pin 1 marking for proper orientation.
	57	Table 21	Footnote added regarding power sequencing.
			MAX specification for Crystal Frequency changed to 20 MHz; Note 3 clarified.
	58	Very Low Temperatures and Noise Immunity	Text regarding operating the device at very low temperatures with an external clock. added.
	62	Power Supply Sequencing	Specifications for power supply sequencing added.
	62	Linear Regulator	Note about using the Linear Regulator to power external devices added.
	63	Table 28	Clarified tIDD for more than one WAIT state, added MAX. value for tOHWE.
	67,68	Figures 15,16	Added data latch point for Memory Read cycles.
	70 – 72	Figures 18 – 19	Moved DMA timing waveforms into the Data Sheet for ease of maintenance and to keep all interface diagrams together in one place.
	70 – 76	Figures 20 – 25	Moved LCD timing waveforms into the Data Sheet for ease of maintenance and to keep all interface diagrams together in one place.

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