3.3V Low Skew 1-to-4 Differential/LVCMOS to LVPECL Fanout Buffer

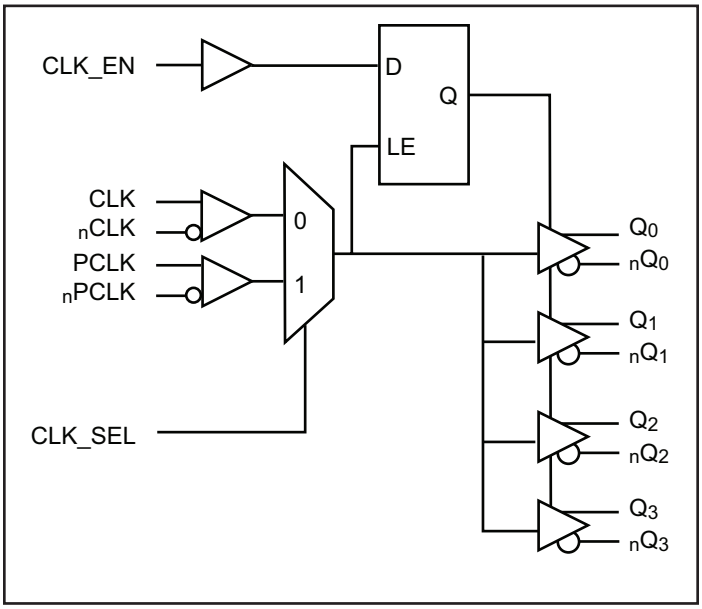
Features

- Pin-to-pin compatible to ICS8533-01
- Maximum operation frequency: 800MHz
- 4 pair of differential LVPECL outputs
- Selectable differential CLK and PCLK inputs
- CLK, $_n$CLK pair accepts LVDS, LVPECL, LVHSTL, SSTL and HCSL input level
- PCLK, nPCLK pair supports LVPECL, CML and SSTL input level
- Output Skew: 100ps (maximum)
- Part-to-part skew: 150ps (maximum)
- Propagation delay: 2ns (maximum)
- 3.3V power supply
- Operating Temperature: -40°C to 85°C
- Packaging (Pb-free & Green avaliable):
  -20-pin TSSOP (L)

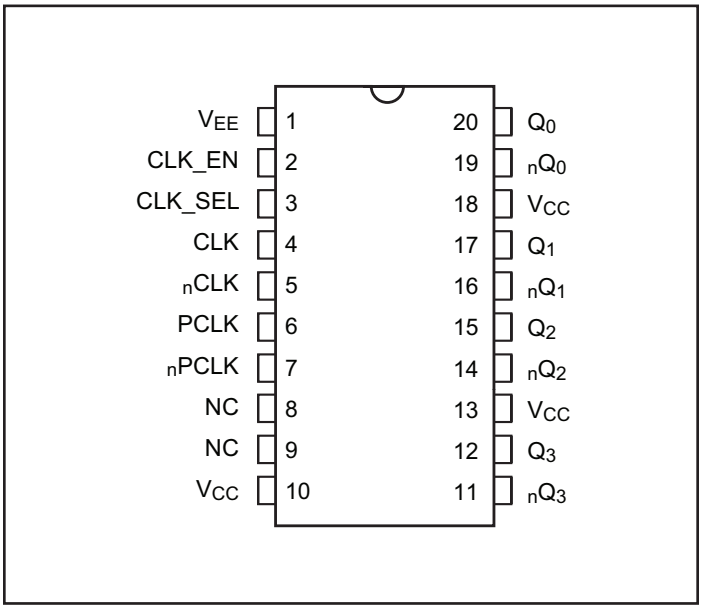
Description

The PI6C48533-01 is a high-performance low-skew LVPECL fanout buffer. PI6C48533-01 features two selectable differential inputs and translates to four LVPECL ultra-low jitter outputs. The inputs can also be configured to single-ended with external resistor bias circuit. The CLK input accepts LPECL or LVDS or LVHSTL or SSTL or HCSL signals, and PCLK input accepts LVPECL or SSTL or CML signals. The outputs are synchronized with input clock during asynchronous assertion/deassertion of CLK_EN pin. PI6C48533-01 is ideal for differential to LVPECL translations and/or LVPECL clock distribution. Typical clock translation and distribution applications are data-communications and telecommunications.

Block Diagram



Pin Diagram



Pin Description

Name	Pin #	Type	Description
V_{EE}	1	P	Connect to Negative power supply
CLK_EN	2	I_PU	Synchronizing clock enable. When high, clock outputs follow clock input. When low, Q_X outputs are forced low, $_nQ_x$ outputs are forced high. LVCMOS/LVTTL level with 50KΩ pull-up.
CLK_ SEL	3	I_PD	Clock select input. When high, selects PCLK input. When low, selects CLK input. LVCMOS/ LVTTL level with 50KΩ pull-down.
CLK	4	I_PD	Non-inverting differential clock input
$_n$CLK	5	I_PU	Inverting differential clock input
PCLK	6	I_PD	Non-inverting differential clock input
$_n$PCLK	7	I_PU	Inverting differential clock input
NC	8, 9		Not connected
V_{CC}	10, 13, 18	P	Connect to 3.3V.
$_nQ_3$, Q_3	11, 12	O	Differential output pair, LVPECL interface level.
$_nQ_2$, Q_2	14, 15	O	Differential output pair, LVPECL interface level.
$_nQ_1$, Q_1	16, 17	O	Differential output pair, LVPECL interface level.
$_nQ_0$, Q_0	19, 20	O	Differential output pair, LVPECL interface level.

Note:
1. I = Input, O = Output, P = Power supply connection, I_PD = Input with pull down, I_PU = Input with pull up

Pin Characteristics

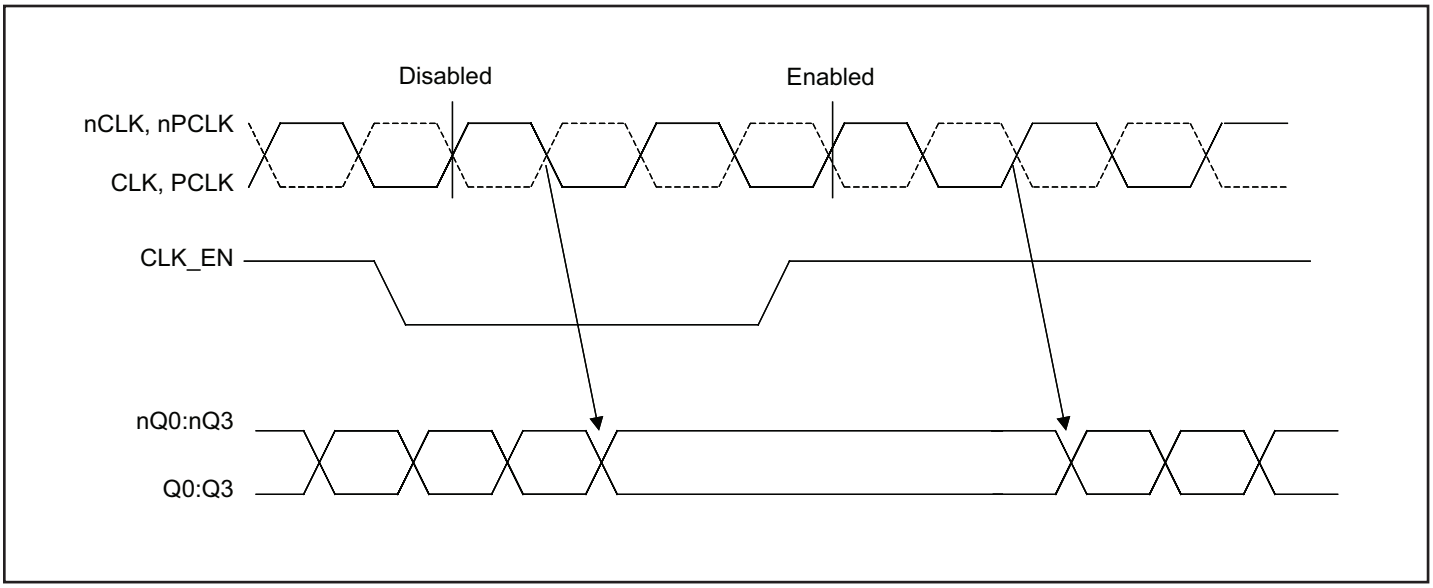
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
C_{IN}	Input Capacitance				4	pF
R_pullup	Input Pullup Resistance			50		KΩ
R_pulldown	Input Pulldown Resistance			50		

Control Input Function Table(1)

Inputs			Outputs	
CLK_EN	**CLK_SEL**	**Selected Source**	**Q_0:Q_3**	**$_nQ_0$:$_nQ_3$**
0	0	CLK, $_n$CLK	Diasbled: Low	Diasbled: High
0	1	PCLK, $_n$PCLK	Disabled: Low	Disabled: High
1	0	CLK, $_n$CLK	Enabled	Enabled
1	1	PCLK, $_n$PCLK	Enabled	Enabled

Note:
1. After CLK_EN switches, the clock outputs are disabled or enabled following a rising and falling input clock edge as show below.

Figure 1. CLK_EN Timing Diagram



Clock Input Function Table

Inputs		Outputs		Input to Output Mode	Polarity
CLK or PCLK	$_n$CLK or $_n$PCLK	Q_0:Q_3	$_nQ_0$:$_nQ_3$		
0	1	LOW	HIGH	Differential to Differential	None Inverting
1	0	HIGH	LOW	Differential to Differential	None Inverting
0	Biased; $V_{IN} = V_{CC}/2$	LOW	HIGH	Single Ended to Differential	None Inverting
1	Biased; $V_{IN} = V_{CC}/2$	HIGH	LOW	Single Ended to Differential	None Inverting
Vcc/2	0	HIGH	LOW	Single Ended to Differential	Inverting
$V_{CC}/2$	1	LOW	HIGH	Single Ended to Differential	Inverting

Absolute Maximum Ratings(1)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{CC}	Supply voltage	Referenced to GND			4.6	V
V_{IN}	Input voltage	Referenced to GND	-0.5		V_{CC}+0.5V	
V_{OUT}	Output voltage	Referenced to GND	-0.5		V_{CC}+0.5V	
T_{STG}	Storage temperature		-65		150	°C

Note:
1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress speci fications only and correct functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Operating Conditions

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{CC}	Power Supply Voltage		3.0	3.3	3.6	V
T_A	Ambient Temperature		-40		85	°C
I_{EE}	Power Supply Current	500 MHz			60	mA

LVCMOS/LVTTL DC Characteristics (T_A = -40°C to 85°C, V_{CC} = 3.0V to 3.6V unless otherwise stated.)

Symbol	Parameter		Conditions	Min.	Typ.	Max.	Units
V_{IH}	Input High Voltage			2		V_{CC}+0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	
I_{IH}	Input High Current	CLK, CLK_SEL	V_{IN} = V_{CC} = 3.6V			150	µA
		CLK_EN	V_{IN} = V_{CC} = 3.6V			5	
I_{IL}	Input Low Current	CLK, CLK_SEL	V_{IN} = 0V, V_{CC} = 3.6V	-5			
		CLK_EN	V_{IN} = 0V, V_{CC} = 3.6V	-150			

Differential DC Input Characteristics (T_A = -40°C to 85°C, V_{CC} = 3.0V to 3.6V unless otherwise stated.)

Symbol	Parameter		Conditions	Min.	Typ.	Max.	Units
I_{IH}	Input High Current	$_n$CLK, $_n$PCLK	V_{IN} = V_{CC} = 3.6V			5	µA
		CLK, PCLK	V_{IN} = V_{CC} = 3.6V			150	
I_{IL}	Input Low Current	$_n$CLK, $_n$PCLK	V_{CC} = 3.6V, V_{IN} = 0V	-150			
		CLK, PCLK	V_{CC} = 3.6V, V_{IN} = 0V	-5			
V_{PP}	Peak-to-peak Voltage			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage(1, 2)			V_{EE}+0.5		V_{CC}-0.85V	

Notes:
1. For single ended applications, the maximum input voltage for CLK and nCLK is V_{CC}+0.3V
2. Common mode voltage is defined as V_{IH}.

LVPECL DC Characteristics

(T_A = -40°C to 85°C, V_{CC} = 3.0V to 3.6V, R_L= 50Ω to V_{CC} - 2V, unless otherwise stated below.)

Symbol	Parameter		Conditions	Min.	Typ.	Max.	Units
I_{IH}	Input High Current	$_n$CLK, $_n$PCLK	$V_{IN} = V_{CC}$ = 3.6V			5	µA
		CLK, PCLK	$V_{IN} = V_{CC}$ = 3.6V			150	
I_{IL}	Input Low Current	$_n$CLK, $_n$PCLK	V_{CC} = 3.6V, V_{IN} = 0V	-150			
		CLK, PCLK	V_{CC} = 3.6V, V_{IN} = 0V	-5			
V_{PP}	Peak-to-peak Voltage			0.3		1	V
V_{CMR}	Common Mode Input Voltage; Note(1,2)			V_{EE}+1.5		V_{CC}	
V_{OH}	Output High Voltage			V_{CC}-1.4		V_{CC}-0.9	
V_{OL}	Output Low Voltage			V_{CC}-2.0		V_{CC}-1.6	
V_{SWING}	Peak-to-peak Output Voltage Swing			0.6		1.0	

Notes:
1. For single ended applications, the maximum input voltage for PCLK and $_n$PCLK is V_{CC}+0.3V.
2. Common mode voltage is defined as V_{IH}.

AC Characteristics(1) (T_A = -40°C to 85°C, V_{CC} = 3.0V to 3.6V, R_L= 50Ω to V_{CC} - 2V, unless otherwise stated below.)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
f_{max}	Output Frequency			500	800	MHz
t_{Pd}	Propagation Delay(2)		1.0		2.0	ns
Tsk(o)	Output-to-output Skew(3)				100	ps
Tsk(pp)	Part-to-part Skew(4)				150	
t_r/t_f	Output Rise/Fall time	20% - 80%	75		300	
odc	Output duty cycle		40		60	%
J_{add}	Additive Jitter			50		fs

Notes:
1. All parameters are measured at 500MHz unless noted otherwise
2. Measured from the V_{CC}/2 of the input to the differential output crossing point
3 Defined as skew between outputs at the same supply voltage and with equal load condition. Measured at the outputs differential crossing point.
4. Defined as skew between outputs on different parts operating at the same supply voltage and with equal load condition. Measured at the outputs differential crossing point.

Applications Information

Wiring the differenctial input to accept single ended levels

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = V_{CC}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to postion the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{CC} = 3.3V, V_REF should be 1.25V and R1/R2 = 0.609.

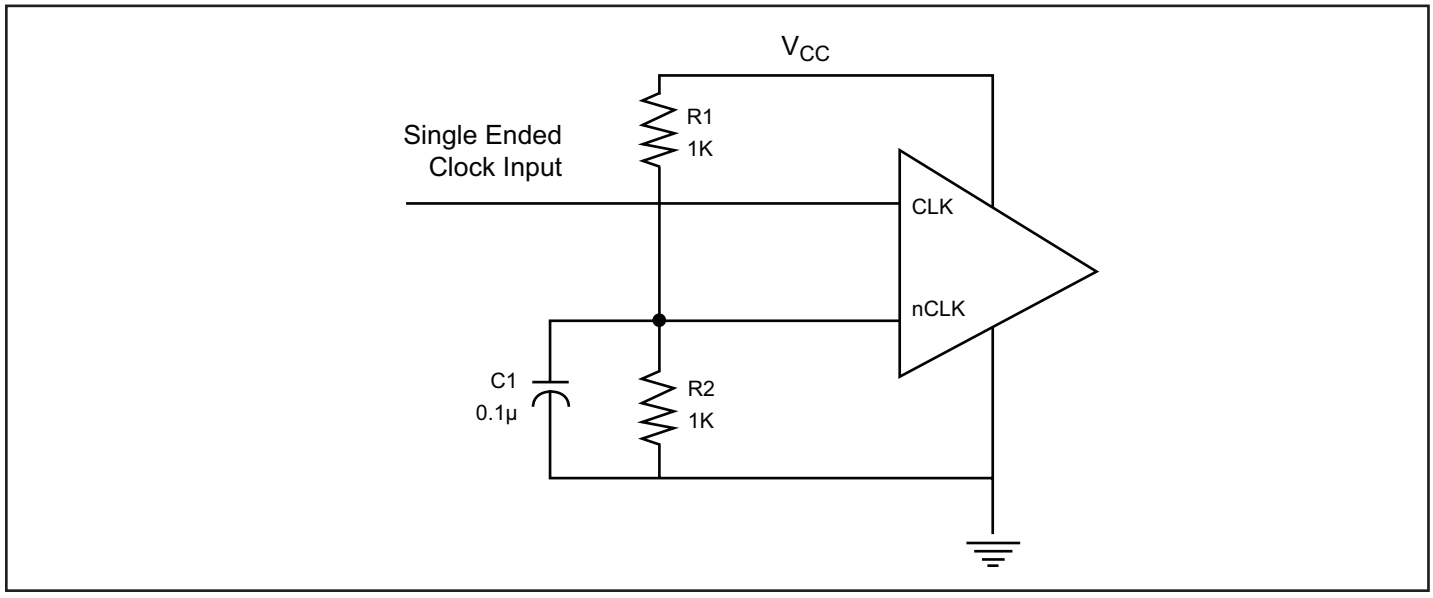
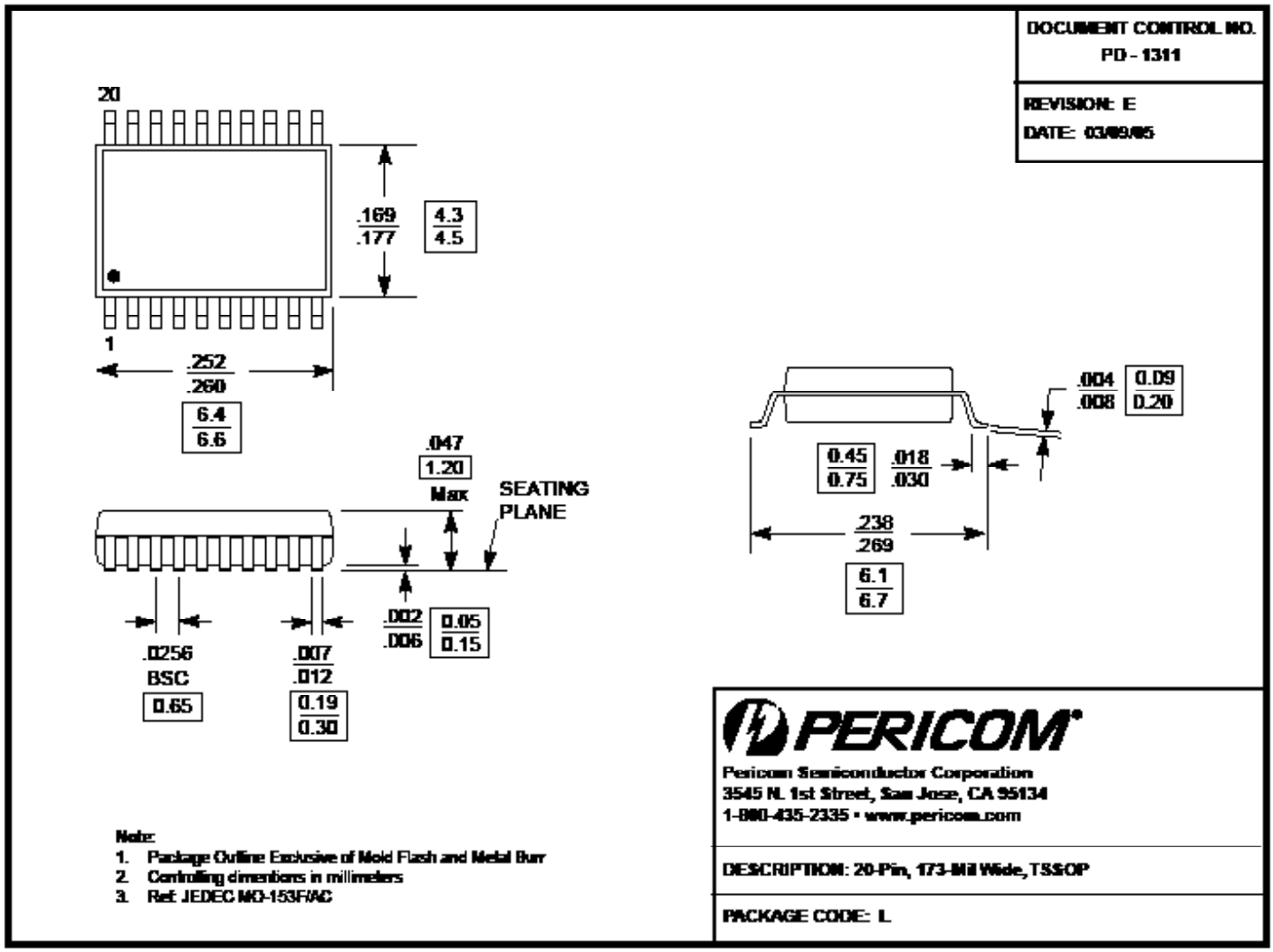


Figure 2: Single-ended Signal Driving Differential Input



Note:
- For latest package info, please check: http://www.pericom.com/products/packaging/mechanicals.php

Ordering Information(1,2)

Ordering Code	Package Code	Package Description
PI6C48533-01LE	L	Pb-free & Green 20-pin 173-mil wide TSSOP
PI6C48533-01LEX	L	Pb-free & Green 20-pin 173-mil wide TSSOP, Tape & Reel

Notes:
1. Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
2. E = Pb-free and Green